Vikash Plytechnic, Bargarh

Vikash Polytechnic
Campus: Vikashknowledge Hub, Barahaguda canal chowk, NH-06
Post/Dist: Bargarh-768028, Odisha

Lecturer Notes on VLSI

Dept : ECE

Sem : 6th

Submitted By : Pankaj Kumar

CONTENTS

UNIT-1: INTRODUCTION TO VLSI & MOS TRANSISTOR

Historical Perspective

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. Typically, the required computational and information processing power of these applications is the driving force for the fast development of this field. Figure 1 gives an overview of the prominent trends in information technologies over the next decade. The current leading edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications for VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example).

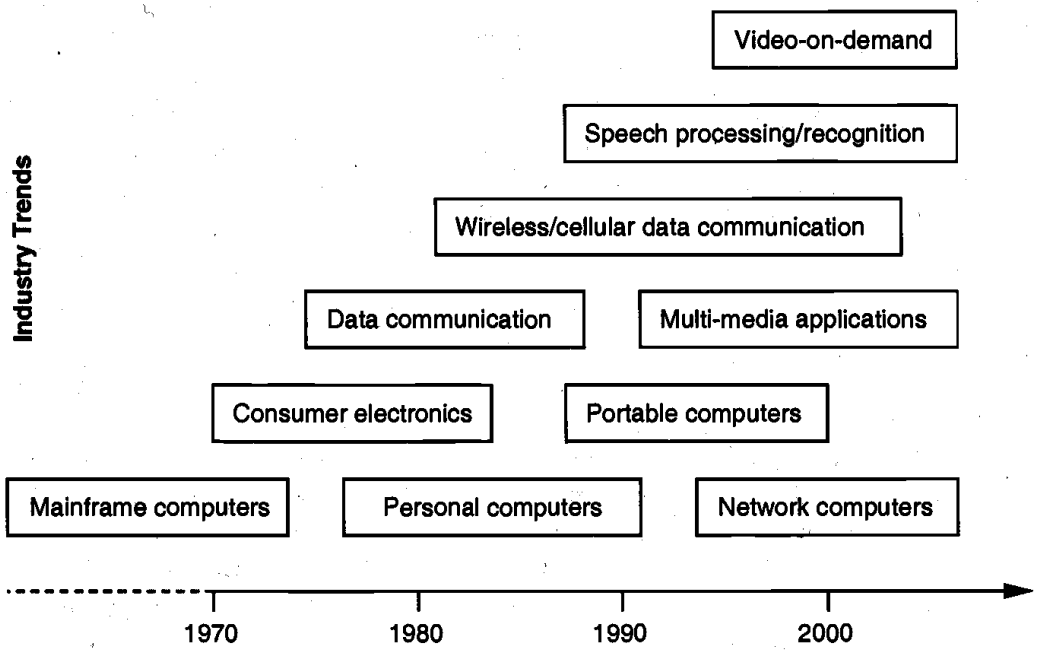


Fig.1.1 Prominent "driving" trends in information service technologies.

Classification of CMOS digital circuit types

ERA	YEAR	COMPLEXITY (#LOGIC BLOCKS PER CHIP)
Single Transistor	1958	Less than 1
Unit Logic (One Gate)	1960	1
Multi Function	1962	2-4
Complex Function	1964	5-20
Medium Scale Integration (MSI)	1967	20-200
Large Scale Integration (LSI)	1972	200-2000
Very Large Scale Integration (VLSI)	1978	2000-20000
Ultra Large Scale Integration (ULSI)	1989	Above 20000

The Metal Oxide Semiconductor (MOS) Structure

We will start our investigation by considering the electrical behaviour of the simple two terminal MOS structure shown in Fig. 1.2 below. Note that the structure consists of three layers: The metal gate electrode, the insulating oxide (SiO2) layer, and the p-type bulk semiconductor (Si), called the substrate. As such, the MOS structure forms a capacitor, with the gate and the substrate acting as the two terminals (plates) and the oxide layer as the dielectric. The thickness of the silicon dioxide layer is usually between 10 nm and 50 nm. The carrier concentration and its local distribution within the semiconductor substrate can now be manipulated by the external voltages applied to the gate and substrate terminals. A basic understanding of the bias conditions for establishing different carrier concentrations in the substrate will also provide valuable insight into the operating conditions of more complicated MOSFET structures.

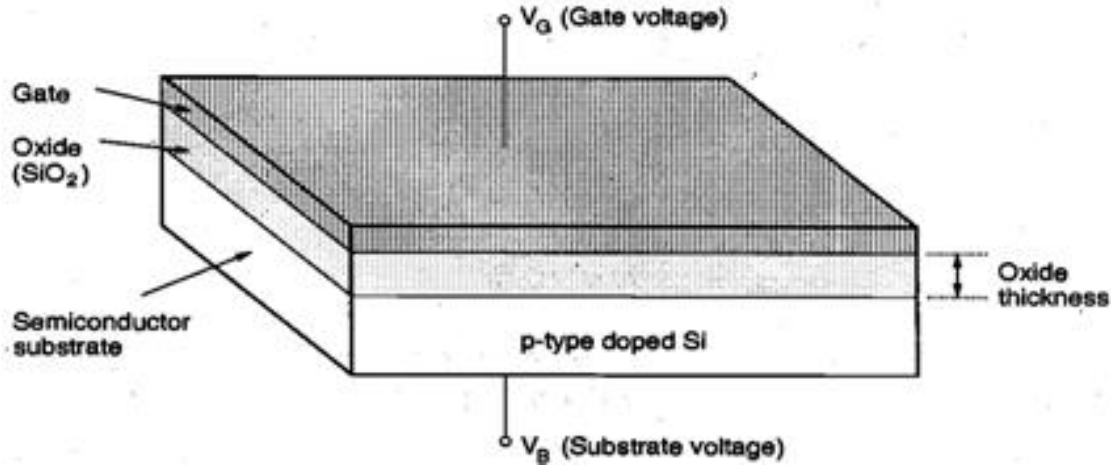


Fig. 1.2 Simple two terminal MOS structure shown in

N-MOS transistor

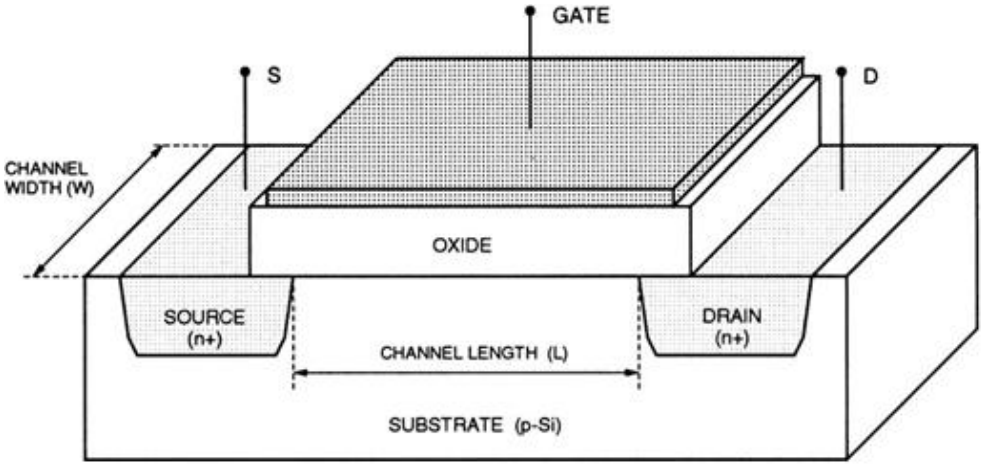


Fig 1.3 Structure of an N-channel MOSFET

- The basic structure of an N-channel MOSFET is shown in the fig 1.3 above.
- It is a 4 terminal device consisting of P-type substrate in which 2 N^+ diffusion regions (the drain and source) are formed.
- The surface of the substrate regions between the drain and the source is covered with a thin oxide layer. The metal or poly silicon gate is deposited on top of the dielectric.
- The distance between the drain and source diffusion regions is known as the channel length.
- The lateral extent of the channel (perpendicular to channel length) is the channel width.

Modes of operation

- A MOS transistor with no conducting channel at zero gate bias is known as enhancement type MOSFET.
- If a conducting channel already exists at zero gate bias, the device is known as depletion type MOSFET.

In an N-channel MOSFET, the source is the N^+ region which has a lower potential in between the 2 layers.

Operation (Enhancement type):

- The simple operating principle of the device is to control the current in the channel between source and drain by varying the electric field at the gate terminal.
- For small gate voltage levels, the majority carriers of the substrate (holes) are repelled back into the substrate and the surface of the P-type substrate is depleted. Since the surface

is not having any mobile carriers current conduction between source and drain is not possible.

- When the gate-source voltage is further increased and the surface potential reaches the threshold level, surface inversion will take place resulting formation of a N-layer below the surface between source and drain.
- This channel now provides an electrical path between source and drain which establish the current flow as long as there exist a potential difference between source and drain terminal.
- The value of gate-source voltage required for surface inversion is known as threshold voltage (V_{th}).
- Any gate-source voltage less than 'V_{th}' is not sufficient to establish the surface inversion layer. Thus the MOSFET can't conduct below the threshold potential.
- When the gate-source potential is above the threshold level, the channel width increases to certain extent then it saturates. Thereafter with increase in gate-source voltage, the channel width remains constant and a constant current flows between the source and drain known as 'saturation current'.

Operation (Depletion type):

- The simple operating principle of the device is to control the current in the channel between source and drain by varying the electric field at the gate terminal.
- In this case the channel is already present between source and drain. Hence at zero gate bias voltage, the current flows between source and drain. Hence in order to control the drain current the applied gate voltage is to be (- ve).
- When the negative gate-source voltage is applied the channel width is reduced and also the current through the channel.
- At certain reverse gate potential the channel is totally truncated and there exists no conducting path between the source and drain. The negative potential at which the channel is cut off and no drain current flows is known as the **Threshold potential (V_{TH})**.
- When the MOSFET is operated at $V_{GS} \geq 0V$, it is said to be in saturated region.
- When the MOSFET is operated at $V_{TH} < V_{GS} < 0$, it is said to be in active/linear region.
- When the MOSFET is operated at $V_{GS} < V_{TH}$, it is said to be in cutoff region.

MOSFET current equations

- Generalized current equation
  - $I_D=(\mu_n C_{ox} W/2L)\{[2(V_{GS}-V_{TH})V_{DS}]-V_{DS}^2\}$
- Active/linear region operation [$V_{DS}<<(V_{GS}-V_{TH})$]
  - $I_D=(\mu_n C_{ox} W/L)[(V_{GS}-V_{TH})V_{DS}]$
  - $R_{CHANNEL}=V_{DS}/I_D=L/[(\mu_n C_{ox} W)(V_{GS}-V_{TH})]$

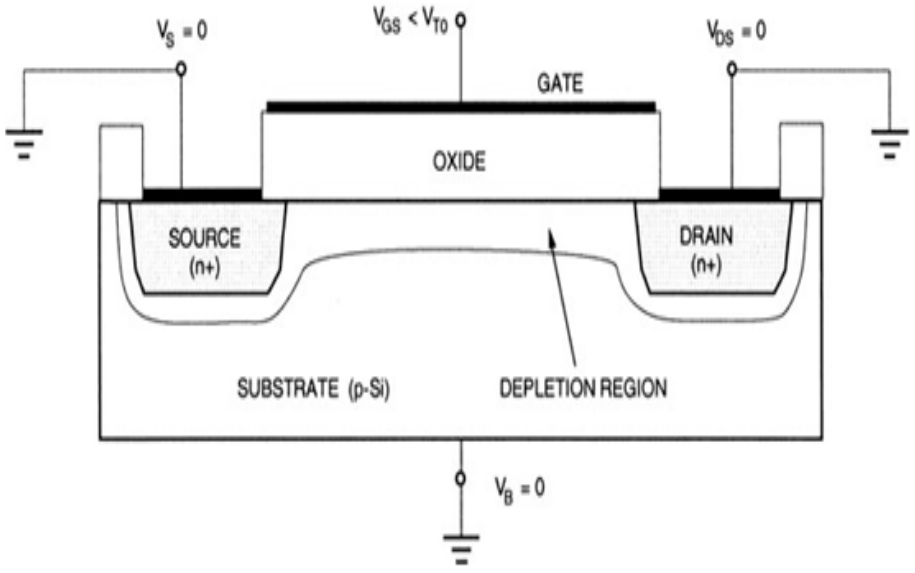
In this case the MOSFET acts as a voltage dependent linear resistor. The channel resistance increases with increase in the channel length and decreases with the increase in the channel width. Under this condition the MOSFET is said to be operating in linear/ active region.

- Saturation region operation[$V_{DS}\geq(V_{GS}-V_{TH})$]
  - $I_D=(\mu_n C_{ox} W/2L)(V_{GS}-V_{TH})^2$

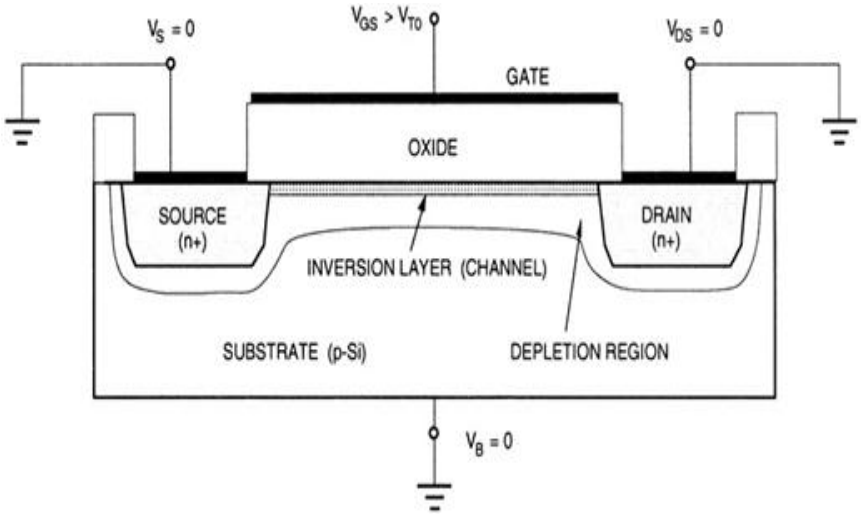
When $V_{DS}=(V_{GS}-V_{TH})$, the gate to channel voltage drop V_{GC} at the drain end is given by

$$V_{GC}=V_{GS}-V_{DS}=V_{GS}-(V_{GS}-V_{TH})=V_{TH}$$

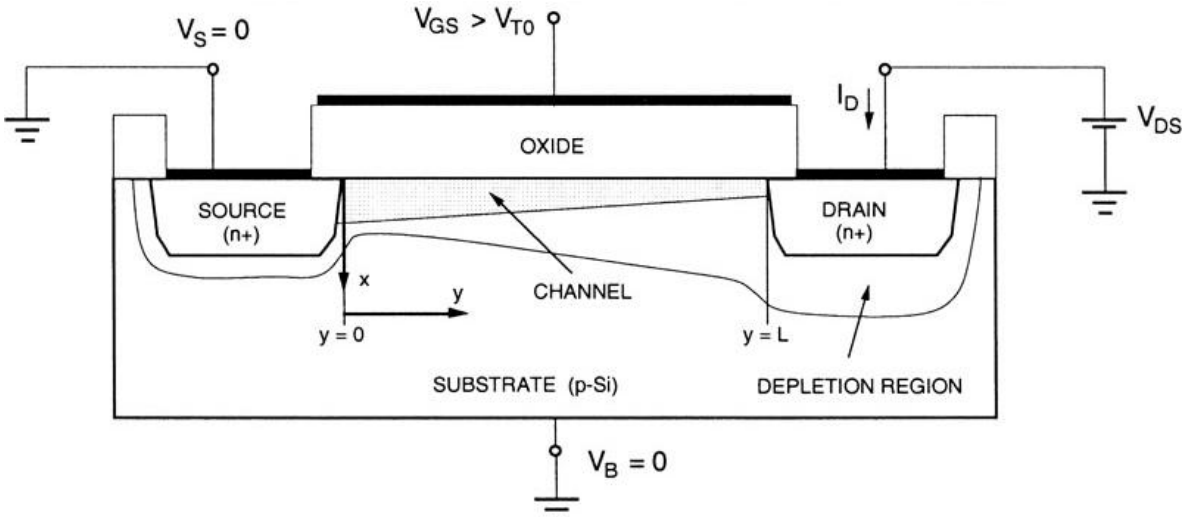
Hence, the inversion layer just begins to disappear at the drain end. Under this condition the channel is pinched off. The drain current remains constant and the transistor operates under saturation region.



(i) Cut-off Region



(ii) Active region operation



(iii) Saturation region of operation

(iv)

Fig. 1.4 Operating regions of N-Channel MOSFET

V-I characteristics of MOSFET

- The V-I characteristic shows the variation of drain current with the change in source-drain potential (V_{ds}) at constant value of gate-source voltage (V_{gs}).
- The drain current is given by:

$$I_d = \frac{\mu_n \, Cox \, W}{2L}\{[2(Vgs - Vto)Vds] - \mathrm{Vds}^2\}$$

Where

μ_n= Charge carrier mobility L= Channel Length V_{ds}= Drain-source voltage

Cox= Oxide layer capacitance V_{gs}= Gate –source voltage

W= Channel width V_{th}= Threshold voltage

- Considering the ideal operating conditions

$$I_d \alpha k (V_{ds} - V_{ds}^2)$$

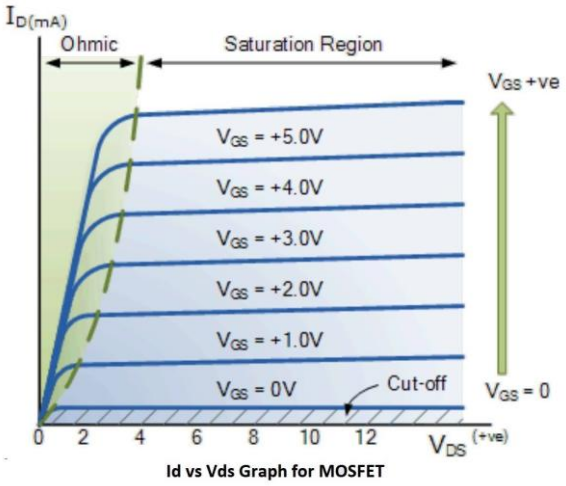


Fig. 1.6 V-I Characteristics of MOSFET

The above Fig. 1.6 represents the variation in I_d with the change in V_{ds} at different V_{gs}. From the above characteristic plot the following points may be summerised:

1. Below certain value of the Gate-Source potential, the channel does not exist between Source and drain region and the transistor operates in the cutoff mode.
2. At certain positive gate potential $V_{gs} = V_{th}$ the channel is formed uniformly between source and drain, as a result the MOSFET exhibits resistive mode of operation on application of V_{ds}.
3. increases linearly up to V_{th}, there after the I_d becomes constant i.e. saturation current flows through the channel.

MOSFET capacitances:

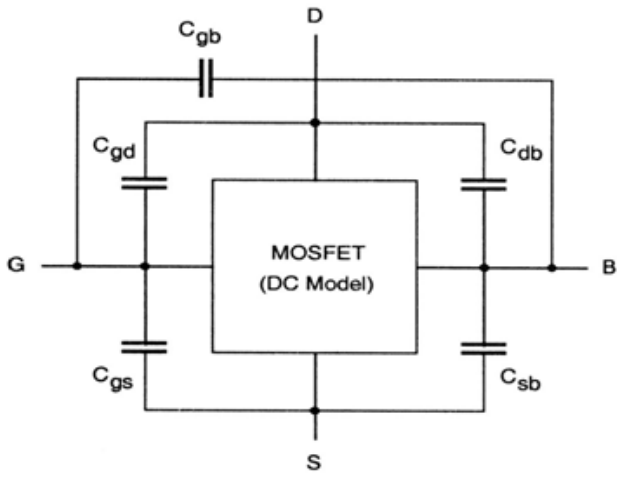


Fig. 1.7 MOSFET Capacitances

The parasitic device capacitances as shown in Fig 1.7 can be broadly classified into two major groups

- Oxide related capacitance
- Junction capacitance

➢ Oxide related capacitance:

- In these capacitors the gate oxide acts as the dielectric. Hence C_{GS}, C_{GD}, C_{GB} capacitors are included in this group.
- The behavior of these capacitors can be examined under 3 operating conditions of the MOSFET.
- Assuming the source and gate diffusion regions have same width 'W' and gate-source, gate-drain overlapping region length be 'L_D', the overlapping capacitance can be represented by

$$C_{GB}\,(\text{overlap}) = C_{GD}(\text{overlap}) = C_{ox} L_D W$$

Where C_{OX} is the junction capacitance per unit area and is given by 'ε/t'

'ε' is the dielectric constant of the oxide layer.

't' is the thickness of the oxide layer.

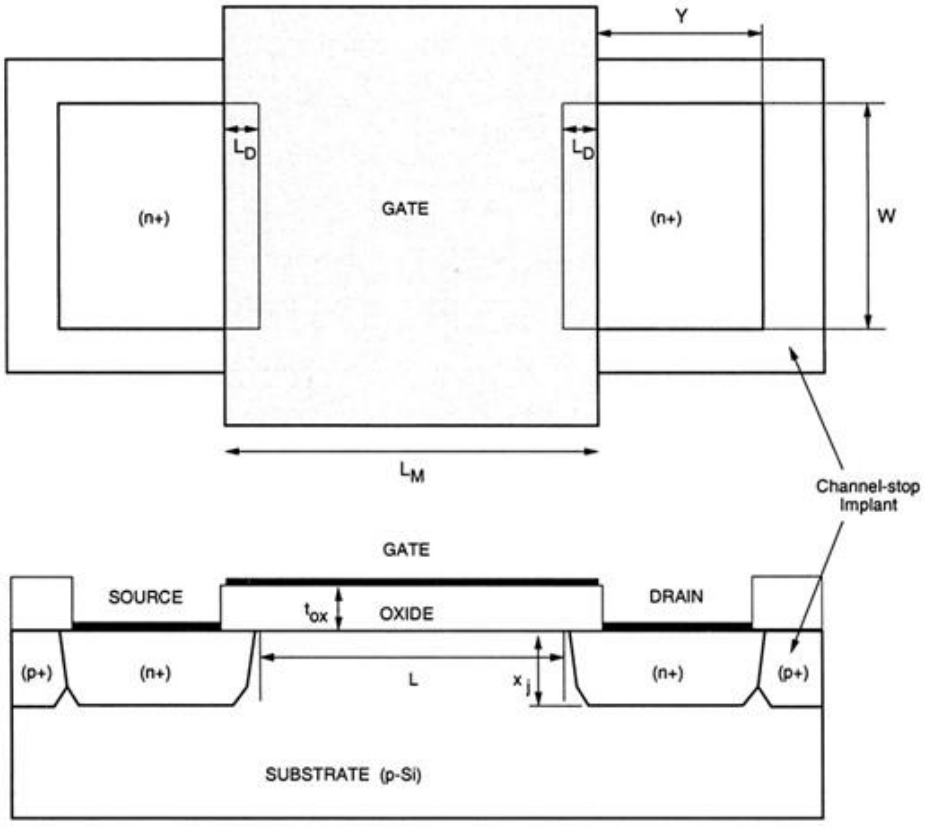


Fig. 1.8 Oxide related Capacitances

- Both these capacitors are not depending on the biasing conditions.
- In the cutoff mode, there is no conducting channel between source and drain. Hence $C_{GS}= C_{GD}=0$ and $C_{GB}= C_{ox}L_DW$
- In the active mode of operation the conducting channel connects the source and the drain. Hence $C_{GB}=0$ and the total capacitance is shared between the source and drain is given by '$C_{GS}= C_{GD}= C_{ox}L_DW/2$'.
- In the saturation mode of operation, the channel is pinched off. Hence '$C_{GD}=C_{GB}=0$' and $C_{GS} \approx ⅔C_{ox} L_DW$
- The total value of junction capacitance reaches the minimum value ($\approx ⅔C_{ox} L_DW$)in saturation mode and maximum value($C_{ox}L_DW$) in cutoff mode.

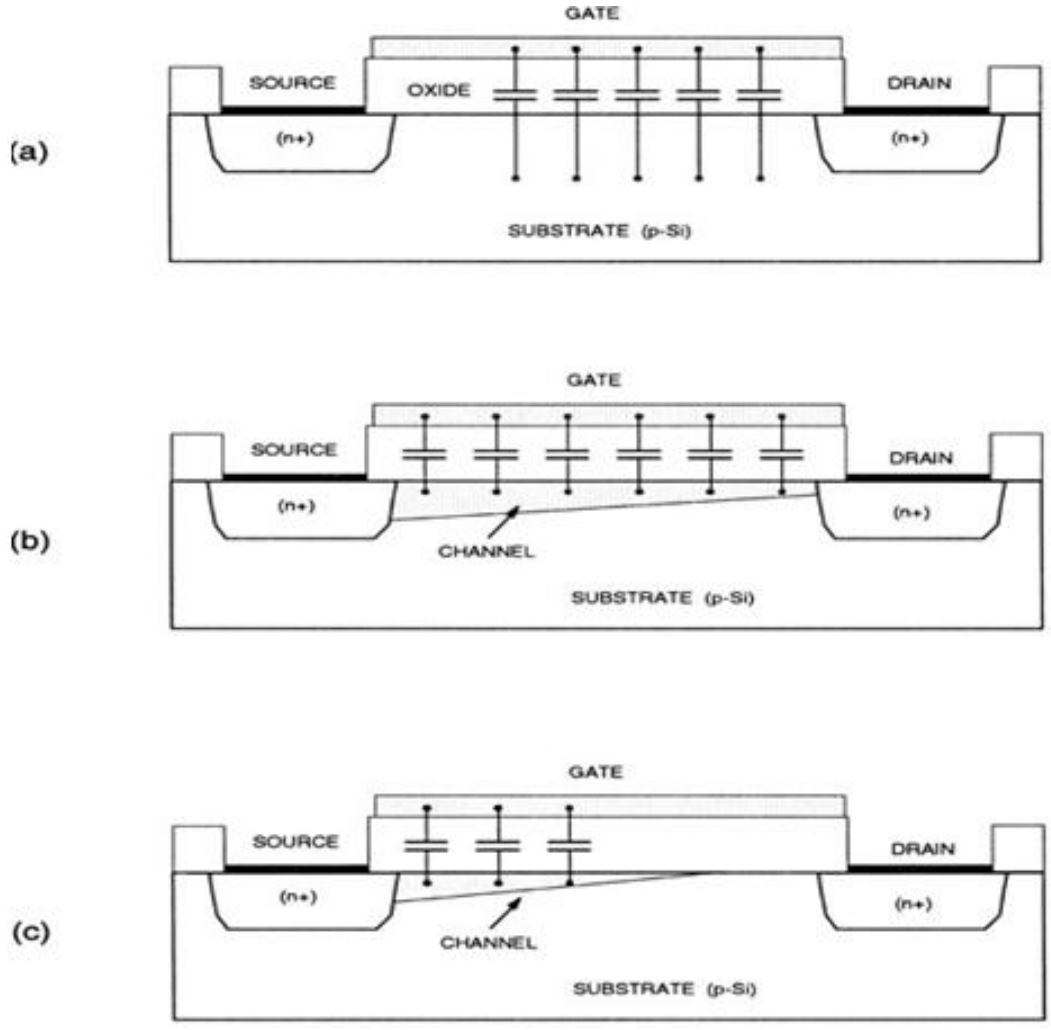


Fig. 1.9 Capacitance distribution based on channel condition

- Junction capacitance:

- The capacitance formed by P-N junction depletion region in the MOSFET are known as junction capacitances.(C_{SB} & C_{DB}) are included in this group. Both these capacitances are due to the depletion charge surrounding the respective source and drain diffusion regions in the substrate.
- Both the junctions are reverse biased under normal operating conditions and the junction capacitance is dependent on the applied terminal voltages.
- The depletion layer capacitance again has two components: one is due to bottom wall and other due to side wall.
- The capacitance due to bottom wall is given by $C_{jb} = C_j W L_s = C_J W L_D$
- The capacitance due to side wall is given by $C_{JSW} = C_{JS} X_j (W+2L_S) = C_{JS} X_j (W+2L_D)$
- Hence the total junction capacitance is given by

$C_{SJN}=C_{JB}$ * Area $+C_{JSW}$ * Perimeter

$=C_{JB} W L_S+C_{JSW} (2L_S + W) + C_{JB} W L_D+C_{JSW} (2L_D + W)$

Where, C_J = Vertical junction capacitance per unit area

C_{JS} = Side wall junction capacitance per unit length

L_S = length of source region

L_D = length of drain region

W = width of source and drain region

Modeling of MOS Transistors including Basic concept the SPICE level-1, level-2 and level-3 model

The LEVEL 1 Model Equations

The LEVEL 1 model is the simplest current-voltage description of the MOSFET, which is basically the GCA-based quadratic model originally proposed by Shichman and Hodges. The equations used for the LEVEL 1 n-channel MOSFET model in SPICE are as follows.

Linear Region

$$I_D = \frac{k'}{2}\frac{W}{L_{eff}}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2](1 + \lambda V_{DS}) \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \ldots.(1)$$

Saturation Region

$$I_D = \frac{k'}{2}\frac{W}{L_{eff}}[(V_{GS} - V_T)^2](1 + \lambda V_{DS}) \quad \text{for } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T \ldots.(2)$$

where the threshold voltage V_T is calculated as

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\emptyset_F| + V_{SB}} - \sqrt{|2\emptyset_F|}\right)$$

Note that the effective channel length *Le* used in these equations is found as follows:

$$L_{eff} = L - 2L_D$$

The LEVEL 2 Model Equations

To obtain a more accurate model for the drain current, it is necessary to eliminate some of the simplifying assumptions made in the original GCA analysis. Specifically, the bulk depletion charge must be calculated by taking into account its dependence on the channel voltage. Solving the drain current equation using the voltage-dependent bulk charge term, the following current-voltage characteristics can be obtained:

$$I_D = \frac{k'}{(1-\lambda V_{DS})}\frac{W}{L_{eff}}\left\{\left(V_{GS} - V_{FB} - |2\emptyset_F| - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\gamma\left[(V_{DS} - V_{BS} + |2\emptyset_F|)^{3/2} - (-V_{BS} + |2\emptyset_F|)^{3/2}\right]\right\}$$

The saturation voltage V_{DSAT} can be calculated as

$$V_{DSAT} = V_{GS} - V_{FB} - |2\emptyset_F| + \gamma^2\left(1 - \sqrt{1 + \frac{2}{\gamma^2}(V_{GS} - V_{FB})}\right)$$

The saturation mode current is

$$I_D = I_{DSAT}\frac{1}{(1-\lambda V_{DS})}$$

The LEVEL 3 Model Equations

The LEVEL 3 model has been developed for simulation of short-channel MOS' transistors; it can represent the characteristics of MOSFETs quite precisely for channel lengths down to 2 gum. The current-voltage equations are formulated in the same way as for the LEVEL 2 model.

$$I_D = \mu_s C_{ox}\frac{W}{L_{eff}}\left(V_{GS} - V_T - \frac{1+F_B}{2}V_{DS}\right)V_{DS}$$

Where

$$F_B = \frac{\gamma F_S}{4\sqrt{|2\emptyset_F| + V_{SB}}} + F_n$$

The empirical parameter *FB* expresses the dependence of the bulk depletion charge on the three-dimensional geometry of the MOSFET. Here, the parameters *VT, Fs,* and *us* are influenced by the short-channel effects, while the parameter Fn is influenced by the narrow- channel effects. The dependence of the surface mobility on the gate electric field is simulated as follows:

$$\mu_s = \frac{\mu}{1 + \theta(V_{GS} - V_T)}$$

Design Flow Procedure:

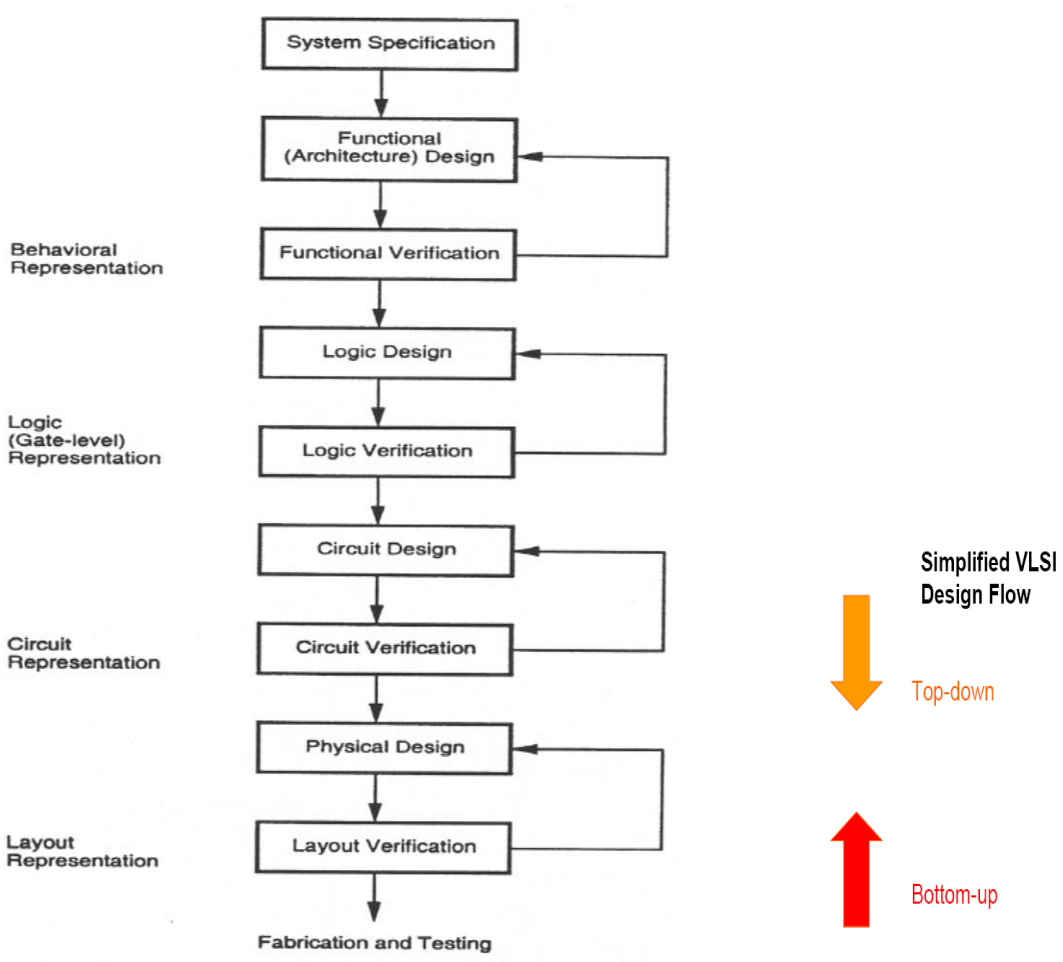


Fig. 1.10 VLSI Design flow

Design Hierarchy:

- In VLSI design the complexity of circuit is very high as there is an involvement of huge number of components in a single IC.
- In order to simplify the design perspective, the main circuit is divided into functional sub modules. This division process into smaller sub circuits is known as the design hierarchy.
- The design hierarchy of a 4 bit binary ripple carry adder circuit is shown in the figure below in which the main circuit is divided in different steps up to component level.

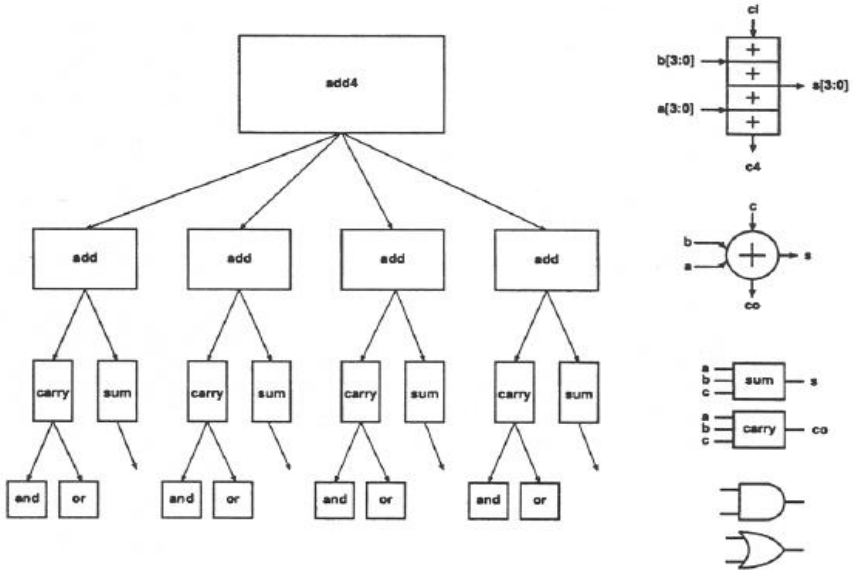


Fig. 1.11 VLSI Design Hierarchy

VLSI Design Flow (Y-Chart):

- The VLSI design flow demonstrates the steps involved in designing a certain circuit on a single chip. There is a need of structured design methodology for designing complex structures. The Y-chart approach demonstrates that approach.
- The VLSI design flow starts with a given set of required parameters. The Y-chart shown in Fig. 1.12 represents the designing procedure of a complex micro processor chip.
- The Y-chart comprises of three domains, namely behavioral domain, structural domain and geometrical lay out domain. In behavioral domain the logic behind the next step implementation is finalized. In structural domain the required components/equipments are decided. In geometrical lay out domain the efficient placement of the circuits/components on the chip is finalized.
- The initial stage is the development of functional components (block level) according to the given specifications. So in the first step the functional block diagram is developed (in behavioral domain) and checked for its proper functionality (in structural domain). Finally the blocks are laid down and inter connected according to the specifications in the design chip area (in geometrical lay out domain).
- In the second phase of designing the logic blocks are to be implemented by logic elements i.e. gates/leaf cells. According to the available logic elements in the library, the functional blocks are implemented by these leaf cells (in structural domain). Then the interconnection according to design specifications done on chip level (in geometrical lay out domain). Then the circuit is verified for desired performance.
- Once the logic level testing is done ,the next step is to design the circuits in component level by using basic components like transistor, resistor, capacitor, etc. once the complete circuit is

ready on the IC floor (in geometrical lay out domain) the final checks were conducted. If all the required parameters were meeting then the final fabrication for market was done.

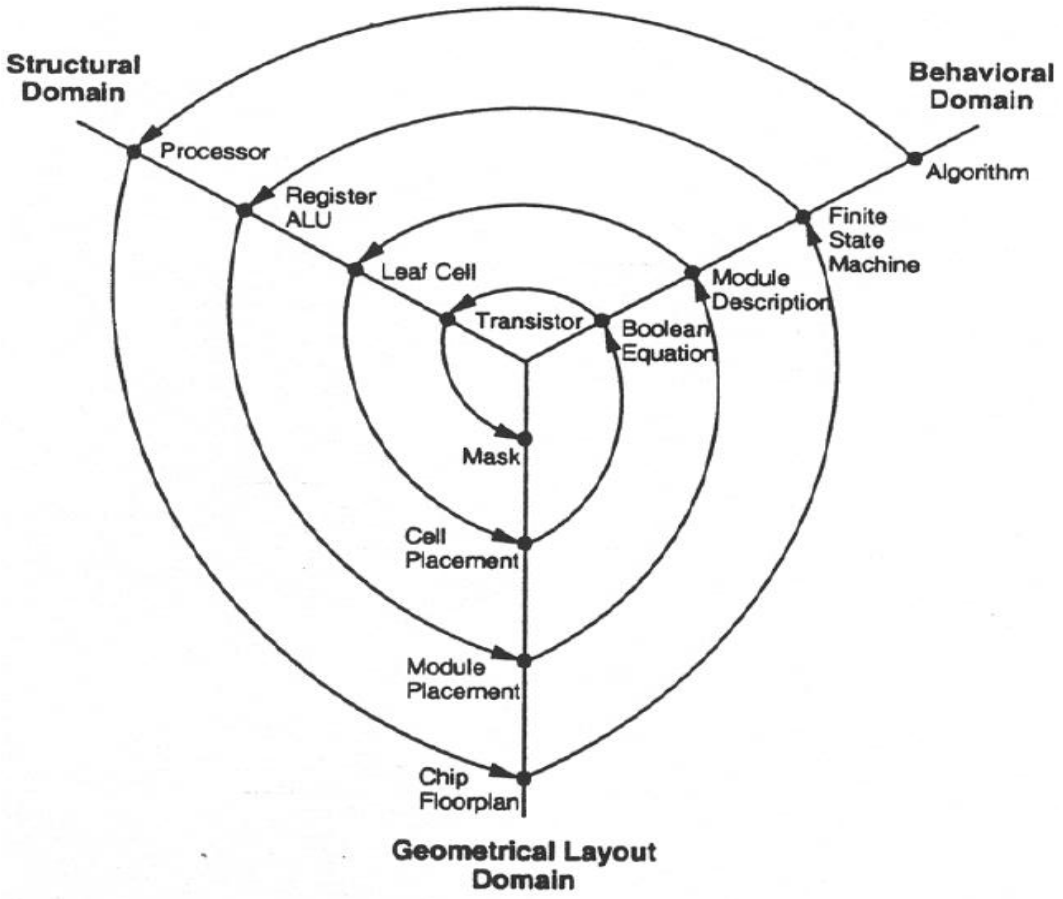


Fig. 1.12 Y-Chart

VLSI Design Styles:

In VLSI the new design may be implemented in different styles such as:

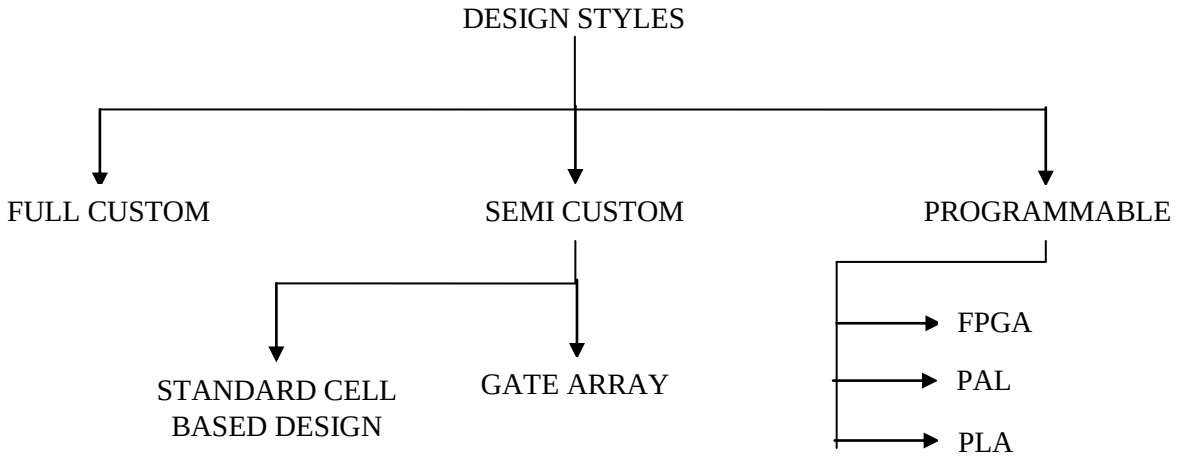


Fig. 1.13 VLSI Design Styles

Field Program gate array (FPGA)

- The FPGA chip contains millions of logic gates having programmable inter connections. The user has to design the hardware for the desired functionality by suitable programming.
- This method provides a means for fast prototyping and for also effective chip design especially for low volume applications.
- A FPGA structure includes I/O buffers, an array of configurable logic blocks and programmable interconnection structure as shown in figure below.
- The programming of the interconnection is accomplished by the programming RAM cells whose output terminals are connected to the gates of MOS transistor. Hence the signal routing between the configurable logic blocks (CLBs) and I/O blocks is accomplished by setting the configurable switches accordingly.
- In this design technology, the architecture is first configured as logic cells available in the chip. Then the CLBs are interconnected by appropriate programming before fabrication. The circuit is checked by using different simulation techniques such as Verilog, VHDL, etc.
- The advantage of FPGA based design is the shortest designing time but it is having higher cost factor than other designing techniques. Hence these are limited for small circuits designing.

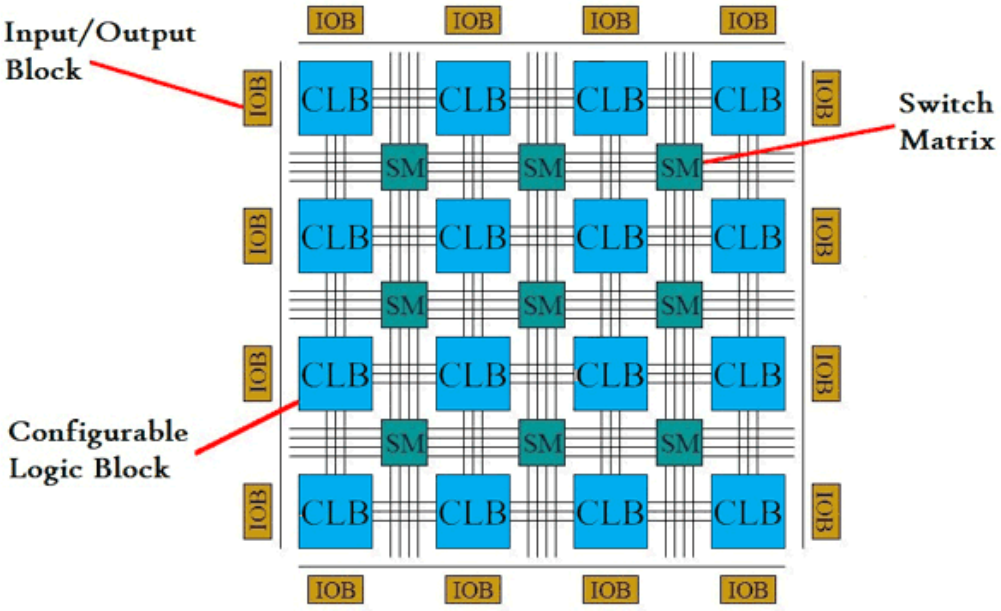


Fig. 1.14 FPGA Structure

Gate Array:

- In terms of prototyping capability, the gate array comes second after the FPGA which has a typical turnaround time of few days.
- The user programming is the core of design implementation in FPGA where as metal mask design and processing is the base for gate array.
- The gate array implementation is a two step process. The first phase which is based on standard mask lay out resulting in an array of uncommitted transistors on each gate array chip. These free uncommitted chips can be stored for later customization. It is accomplished by defining the metal inter connection between the transistors of the array.
- Since the patterning of the metal interconnection is done at the end of chip fabrication process, the turnaround time can be limited from few days to few weeks.
- While most gate array platforms only contain rows of uncommitted transistors separated by routing channels, some other platforms also offer dedicated memory (RAM) arrays to allow higher density where memory functions are required.
- The current gate array chips can implement millions of logic gates on a single chip.

Standard cell based design

- In this design method, the IC uses a set of pre designed, pre tested and pre characterized standard cells.
- The standard cells include basic logic gates, some basic logic structures (adder, multiplexer, encoder, etc), sequential elements (flip-flops, shift registers, etc), I/O buffers, etc are stored in a common library. All these standard cells are designed, tested and characterized for specific functionalities.
- The user makes use of these standard cells to implement his design by simply taking the required modules from the library and interconnecting them.
- In this design style although the design turnaround time is less but there is no scope of performance improvement. Hence the strategy is used for development of less complex commercial products.

Full custom design:

- Here the entire mask design is done without use of any library. However the development cost of such design style is very high. Thus the concept of design reuse is becoming popular in order to reduce design cycle time and development cost.
- The most difficult full custom design is the design of a memory cell. Since the same lay out design is replicated, there is no alternative to high density memory chip design. Whereas for logic chip design, a good compromise can be achieved by using a combination of different design styles on the same chip.
- In real full custom design lay out the geometry, construction, orientation and placement of every transistor is done individually by the designer.
- In this case the design productivity is very low and the designing cost is very high. Hence it is very rarely used for normal circuit designing.
- This method is used only for design of high volume products such as memory chips, high performance microprocessor and FPGA masters.

Semi custom design

- In this style of design, almost all the basic building blocks are used from the standard cell library. Only few cells are designed from the beginning, which are not available in the library or to be optimized for a specific target.
- This approach is faster compared to the full custom style but slower than the standard cell based design.
- Performance wise it is superior to the standard cell based design but inferior to full custom design.

UNIT-2 FABRICATION OF MOSFETS

N-MOS transistor fabrication process

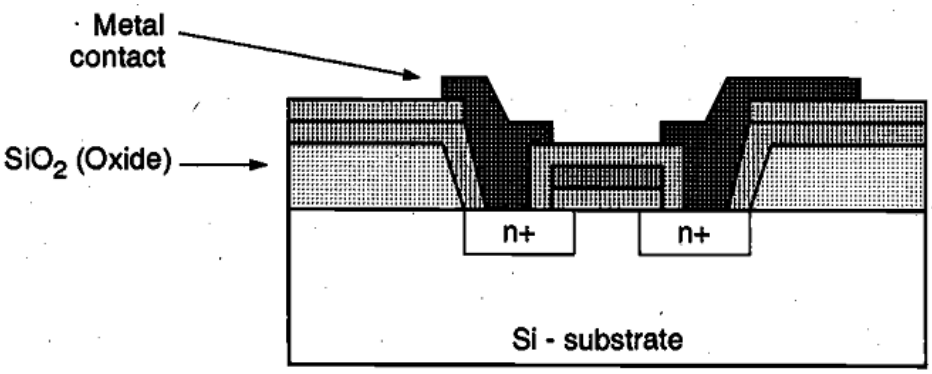


Fig. 2.1 NMOS Transistor Structure

- In NMOS transistor the current flow between two N-type substrates is being controlled by a P-type gate in-order to get signal amplification.
- The figure shows the graphical representation of a NMOS transistor. The step by step fabrication process is given below:
- A P-type material is taken as substrate.
- An oxide layer (SiO_2) is created on the surface of the substrate by oxidation process.
- To create a pattern on oxide layer, a photo resistive material is deposited over the surface of SiO_2 layer. The property of the photo resistive material is that it does not react to the HF acid till it is exposed to ultra violet light.
- The selected portion is to be patternised; the layer of photo resistive material above the selected region is exposed to UV light.
- Hence on application of HF acid, the exposed area photo resistive coating is etched keeping the other area intact.
- Then the SiO_2 layer under uncovered region is etched to expose the substrate.
- Then a resistive thin oxide layer is created on the surface in order to implant the poly silicon gate structure.
- In the next step one more layer of SiO_2 layer is created in order to provide the means to isolate the source, gate and drain structures.
- At the next step in order to create the source and drain region, from the selected portion SiO_2 is removed and pentavalent impurity is added to the exposed surface regions of the substrate. This process creates the N^+ regions as shown in the above figure.
- Finally the metallization process is done to create the source, drain terminals. For the gate terminal metallization is done on the poly silicon gate structure.

CMOS N-well transistor fabrication

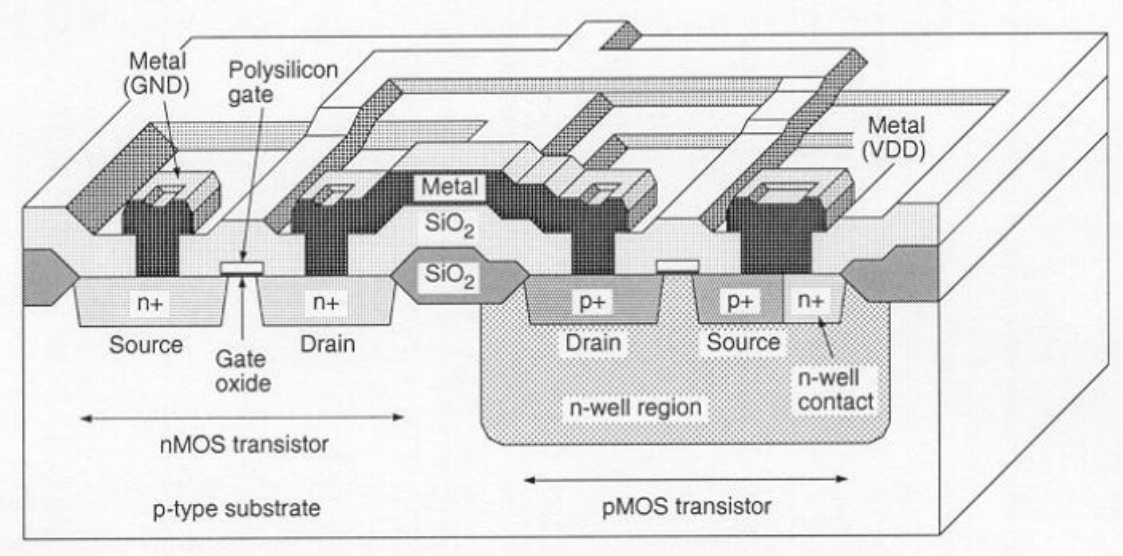


Fig. 2.2 CMOS Transistor circuit

- To fabricate a N-well CMOS transistor, a P-type silicon slab is taken as the base material or substrate. The step by step fabrication process is given below:
- A thick oxide coating is given to the surface of the substrate.
- Then by photo lithographic process, the areas selected for construction of transistors are marked by photo etching process and oxide coating is removed.
- An N-well is created as shown in the figure. There after a thin SiO_2 layer is created known as gate oxide layer. The gate is fabricated at the center of the two transistors by channeling a ploy silicon material as gate.
- Then the thin SiO_2 coating is removed from the transistor surface area and respective impurity is added to create the P^+ and N^+ regions in the silicon slab.
- After creating all the active components of the transistor, a thick SiO_2 layer is created on the surface of the slab as a protective layer.
- Then the SiO_2 top layer is selectively etched in order to facilitate the metallization process for giving the terminal connection between N-MOS NPN transistor and P-MOS PNP transistor as shown in the figure above.

Design Rules

- The physical mask layout of any circuit must confirm to a set of geometric constraints or rules which are generally called layout design rules.

- These rules usually specifies the minimum allowable line width for physical objects on chip such as metal and poly silicon areas, minimum component dimensions, minimum allowable separation between components, etc.

- The design rules can be described in 2 ways
- Micron rule
- Lambda rule

Micron rule: In this the layout constraints such as minimum feature size and their separation are given in absolute dimensions as microns or micrometers.

Lambda Rule: It specifies the layout constraints in terms of a single parameter 'Lambda' and thus allows linear proportional scaling of all geometrical constraints.

Comparison between λ rule and micron rule

λ rule	**micron rule**
Scalable design rules	Absolute design rules
Based on unit λ where λ is the size of minimum feature	Based on absolute distances
Generic for all process technology nodes	Tuned to specific process technology node
Simplified scaling rules	Complex scaling rules specially for deep submicron technology
For each new process technology, λ is reduced keeping the rules same	For each new process technology, rules must be generated fresh
Parasitic are not generally specified in λ units	All geometries are expressed using these rules
Technology migration is easy	Technology migration is difficult
These rules are generally conservative as dimensions are always rounded up to nearest integer that is multiple of λ	These rules are more accurate as all the dimensions are specified in absolute value

Stick diagram:

- It is a simple way of representing the lay out by using thick lines with their inter connections.
- It is useful in estimating the area and planning the layout before the layout is generated within a shorter cycle time.
- The stick diagram shows all the components and their relative placement which helps in planning the lay out and routing.
- It does not show the exact placement of components, transistor size, interconnect length, line width and parasitic elements.
- Lines using different colours used to draw different components of the layout such as red for poly silicon, blue for metal, green for N-diffusion, yellow for P-diffusion and 'X' for contact notification .
- Some thumb rules for drawing the stick diagram are:
  - When same colour lines cross each other they represent an electrical connection.
  - When different colour lines cross each other, there is no electrical contact.
  - When the poly silicon line crosses any of the diffusion line corresponding transistors is represented.
- Few examples of different lay out are given below

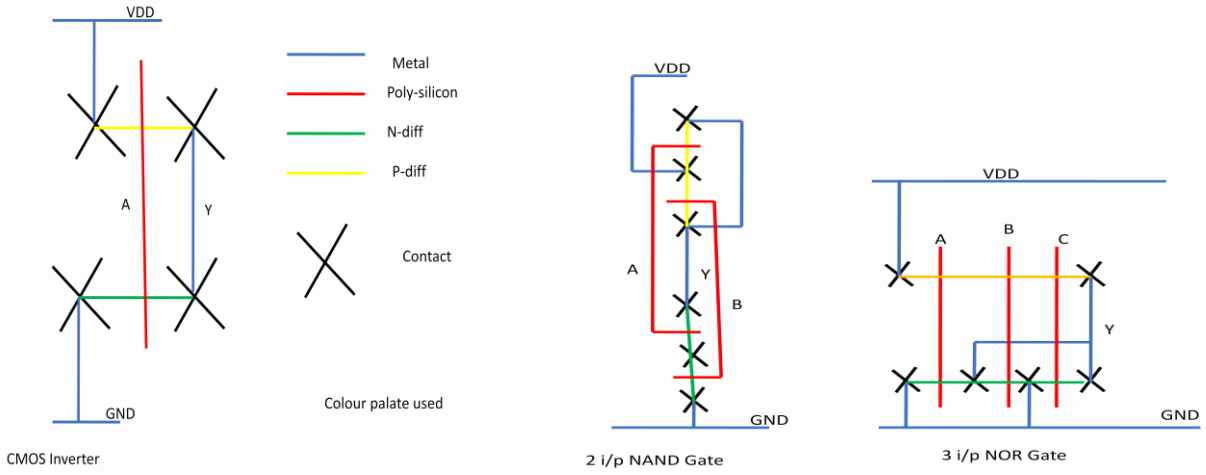
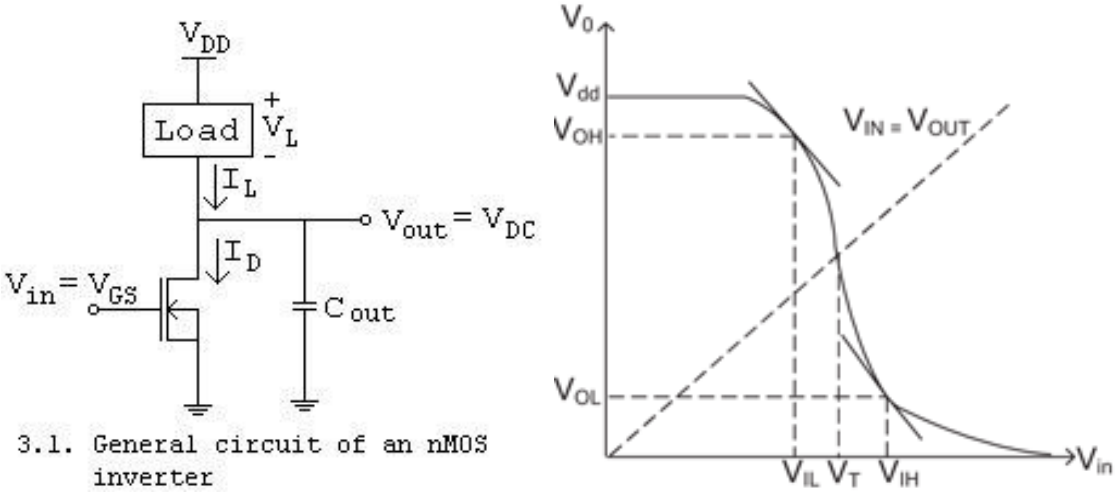


Fig 2.3 Stick Diagram (a) CMOS Inverter (b) 2 i/p NAND Gate (c) 3 i/p NOR Gate

UNIT-3 MOS Inverter

BASIC NMOS INVERTERS



3.1. General circuit of an nMOS inverter

Fig. 3.1 Generalised structure of MOS Inverter with Voltage Transfer Characteristic (VTC)

- The figure 3.1 shows the generalized circuit structure of an N-Channel enhancement type N-MOS inverter with Voltage Transfer Characteristic (VTC) curve.
- The input voltage to the circuit is $V_{in}=V_{gs}$. The output voltage $V_{out}=V_{ds}$.
- The source and the substrate terminals are connected to common ground i.e. $V_{sb}=0$.
- The generalized load is connected between the supplies (V_{dd}) and the drain terminal of driver MOSFET. The characteristic of the inverter depends on the load circuit.
- Since the D.C. gate current of the MOSFET is negligible, there will be no current flow into or out of the input and output terminals of the inverter in D.C. steady state.

OPERATION:-

- For low input voltage levels the output voltage '$V_{out}=V_{cc}=V_{oh}$' as the driver stage is in cut off state and no current flows through the drain circuit, hence no potential drop across the load circuit.
- As V_{in} increases, the driver transistor starts conducting and the output voltage starts reducing. This drop in the output voltage is gradual instead of sharp vertical drop.
- Here two vertical voltage points where the slope '$dV_{out}/dV_{in}=-1$' is shown in the graph as 'V_{IL}' and 'V_{IH}'. Both these voltage plays a significant role in determining the noise margin of the inverter circuits.

- As the input voltage is further increased the output voltage continues to drop and reaches the value 'V_{OL}', when the input voltage is 'V_{OH}'. The inverter threshold voltage 'V_{TH}' is the transition voltage on the graph where '$V_{IN}=V_{OUT}$'.

Resistive Load Inverter

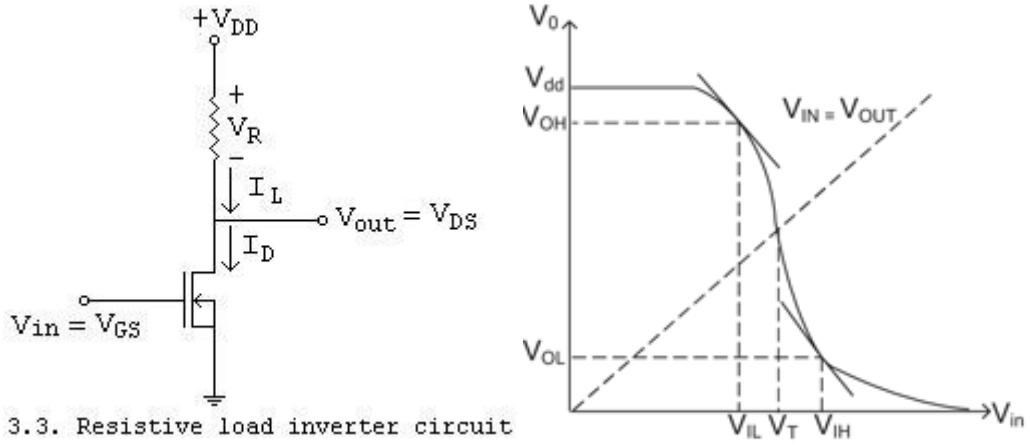


Fig. 3.2 Resistive Load Inverter with VTC

- The figure shows the circuit of a N-channel enhancement type MOSFET inverter with resistive load.
- The load resistors are connected between source potential and drain terminal.
- The current at drain i.e. 'I_D' is equal to the load 'I_R' is in D.C. steady state operation.
- In the circuit the source and the substrate are connected to the common ground.
- The input is applied across gate source terminal. ($V_{gs}=V_{in}$) and the output is taken across the drain source terminal ($V_{out}=V_{ds}$).

OPERATION:-

- For input voltage smaller than threshold voltage, the driver MOSFET is in cutoff state hence '$I_D=0$' and the potential drop across the load resistance '$V_R=0$', so the output potential of the inverter circuit '$V_{out}=V_{cc}$'.
- As the input voltage is increased beyond threshold potential, the driver MOSFET starts conducting. Initially the MOSFET is in saturation region as '$V_{ds} \rangle (V_{in}-V_{th})$'.
- With the increase in input voltage, the drain current of the driver also increases and the output voltage starts reducing. For input voltages more than '$V_{out}+V_{th}$', the driver transistor enters the linear operation region. If the input is further increased the output remains in decreasing mode until it reaches the value 'V_{OL}'.

Inverter with N-MOS Load

- The simple resistive load inverter is not suitable for most digital VLSI system because of the large area requirements for resistive load fabrication, so in these circuits the N-channel MOSs are used as load.
- Depending on the MOSFET type (i.e. enhancement and depletion) the circuit configuration are shown in figure (01) and (02).

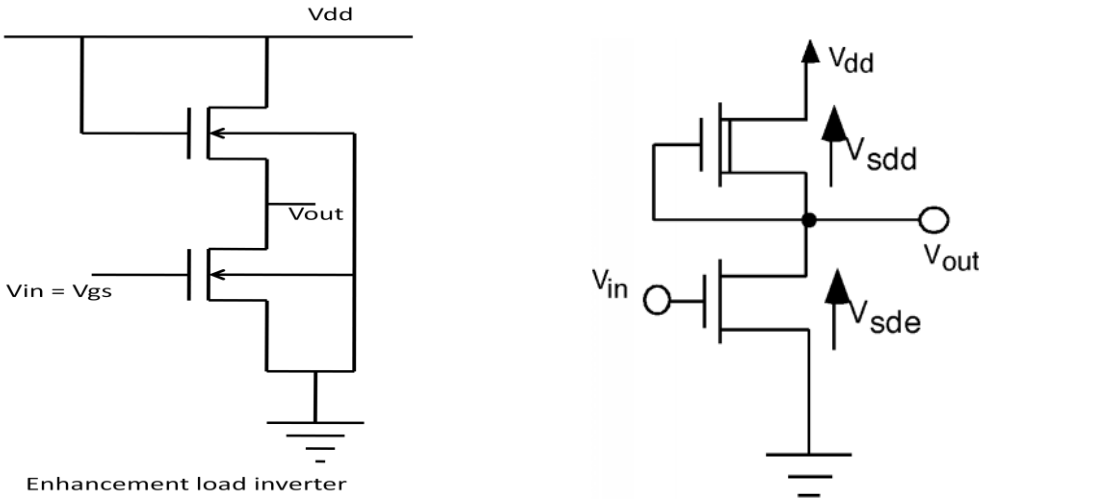


Fig 3.3 NMOS Load Inverter

Enhancement Load N-MOS Inverter

- In this case an enhancement type MOS transistor can be connected as the load to the driver stage.
- The load may be operated either in the saturated region or linear region of operation.
- While operated in saturated region of operation the voltage '$V_{OH}= V_{DD} - V_{th}$'.
- While operated in linear region then $V_{OH}= V_{DD}$.
- The noise margin of linear mode operating load is more than the case of saturated region operating load. Although an additional voltage source required for load MOSFETs at the gate circuit

LIMITATION:-

The inverters suffer from higher noise margins and higher D.C. power dissipation. Hence enhancement load N-MOS inverters are not suitable for large scale digital application.

Depletion Load N-MOS Inverter

- Although the fabrication process of depletion type N-MOS transistor is more complicated than enhancement type, the following advantages are obtained by using depletion load.
- Sharp voltage transfer characteristic transition
- Less noise margin
- Requires single power supply
- Small chip area required

- The figure (02) shows the circuit configuration of a depletion load N-channel MOS inverter.
- Here the driver device use an enhancement type N-MOS transistor (V_{th}>0).
- Whereas the load is depletion type with V_{th}<0. The gate and source terminals of the load are connected hence V_{gs}=0.
- Since the threshold voltage of deletion type loads is negative $V_{gs} > V_{th}$.
- Hence the load device always conducts irrespective of inputs and output voltage levels.
- The operating mode of the transistor is determined by the output voltage level (V_{out}). When V_{out}<V_{dd} +$V_{th,}$ the load transistor is in saturation region and when V_{out}> V_{dd} +V_{th} the load operates in the linear region.

C-MOS Inverter

- The C-MOS inverter circuit consists of an enhancement type N-MOS driver transistor and enhancement type P-MOS transistor in the load circuit.
- Both the transistors operate in the complimentary mode.
- When the input voltage $V_{in} > V_{Th}$, the N-MOS transistor is in conduction state and P-MOS transistor is in cut off state, hence the output potential V_{out}=0.
- When the input voltage $V_{in} < V_{Th}$, the N-MOS transistor is in cut off state and P-MOS transistor is in conduction state, hence the output potential V_{out}=V_{cc}.

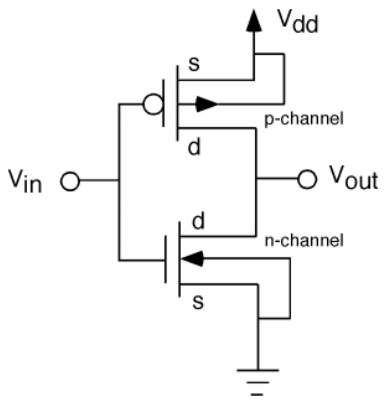


Fig. 3.4 CMOS Inverter

ADVANTAGES:-

The C-MOS inverter is having two important advantages over other inverter configuration.

1. Small steady state power dissipation (D.C.). The small or negligible power dissipation in this case is due to the leakage current only.
2. The voltage transfer characteristic exhibits a full output voltage swing between a zero volt and V_{DD} with a very sharp transition resembling with an ideal inverter characteristic curve and noise margin is reduced.

DISADVANTAGE:-

The fabrication of C-MOS structure is more complex than N-MOS or P-MOS structure. As the N-MOS and P-MOS transistors are fabricated side by side on additional guard ring/separation/insulation must be inserted between the transistors in order to avoid the latch of condition.

Delay time:-

- The input and output voltage wave form of a typical inverter circuit is shown in the figure 3.5.

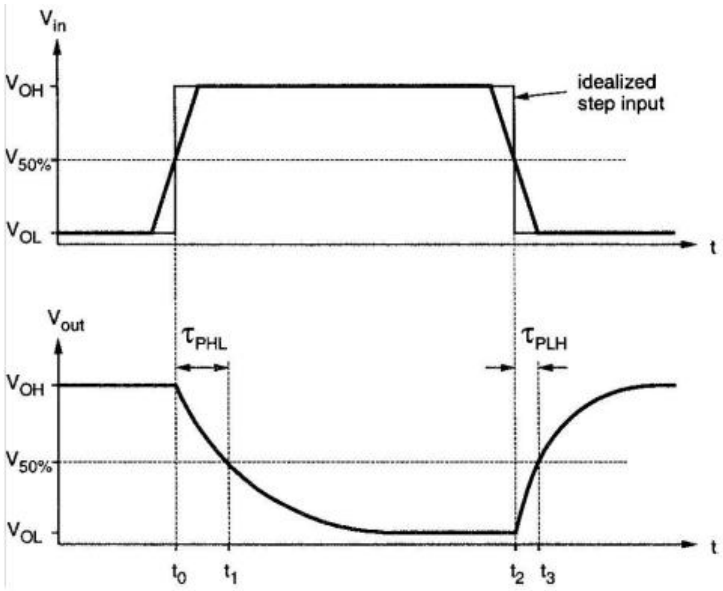


Fig. 3.5 Delay Time in CMOS Operation

- The propagation delay time (T_{phl} and T_{plh}) determines the input to output signal delay during the high to low and low to high transition of the output.
- It is measured at the 50% of the voltage level. The average propagation delay of the inverter characterize the average time required for input signal to propagate through the inverter and is given by-

$$T_P = \frac{Tphl + Tplh}{2}$$

Inverter Design with Delay Constraints

The delay time offered by the MOSFET is due to the capacitors formed during the fabrication process. The following relation gives the dependence of time delay in circuit capacitance.

$$i = C\frac{dV}{dt}$$

$$=> dt = \frac{C}{i}dV$$

$$=> \int dt = \int \frac{C}{i}dV$$

$$=> T = \frac{C}{I}V$$

Hence $T \propto C$

- The load capacitance (C_{load}) consists of intrinsic components (C_{int}) consist of parasitic drain capacitance which depends on transistor dimension and extrinsic capacitance, which consists of interconnecting wiring capacitances and FAN out capacitances which are independent of transistor dimensions.
- In most cases the transistor sizes found from delay requirements must also meet other design criteria such as noise and logic inversion threshold.
- The total capacitive load of the inverter can be experience as:

$$C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$$

Where $\propto_0, \propto_n and \propto_p$ are positive constant coefficients derived by technology-related parameters such as doping densities, minimum channel length and physical geometry (layout design rules) and Wn, Wp are width of N region and P region respectively.

- There exists an limitation to switching speed in C-MOS inverter due to drain parasitic capacitance by increasing 'Wn' and 'Wp' to reduce the propagation delay will have a very little effect on delay beyond certain limiting values which depends the technology related parameter such as doping density, minimum channel length, minimum layout design rules etc.

- If the extrinsic component dominates the total load capacitance, then delay reduction can be achieved for wider range of Wn and Wp and if, intrinsic component is dominant, the speed limit reaches for smaller values of Wn and Wp.
- Due to minimization of the circuits in modern C-MOS technology, the intrinsic gate delays tend to decrease significantly and length of the interconnect line increases due to increase in dense fabrication of the components. In order to achieve high density fabrication the width of the interconnect lines decreases where as the thickness increases, which leads to signal coupling between adjacent lines. The following figure shows the function of the gate delay and interconnects delay with respect to minimization of component size.

Fig 3.6 Delay considerations

UNIT-4 STATIC COMBINATIONAL, SEQUENTIAL AND DYNAMIC LOGIC CIRCUITS

Static and Dynamic Logic Circuits:

- A static logic gate is one that has a well defined output once the inputs are stabilized. Here the switching transients are not considered. If the inputs are well defined then the outputs are also well defined at all times. It does not require clock pulses for refreshing the voltage levels of the nodes. These are reliable easy to design and easy to operate. It is characterized by maximum output swing, noise immunity, no static power dissipation etc. But these circuits offer a large capacitance due to involvement of large number of transistors causing more dynamic power dissipation and propagation delay.
- A dynamic logic gate is one whose output is only valid for a short time period after result is produced. Here the logic is stored as charge at nodes with parasitic capacitances. The logic state is defined by the voltage level or the amount of charge stored at the node. These nodes are to be periodically refreshed by a clock signal to maintain the charge level. These require less number of transistors to construct the circuit. Hence more complex circuits can be implemented in less chip area. They are characterized by higher switching speed and less power consumption.

C-MOS NOR2 Gate:

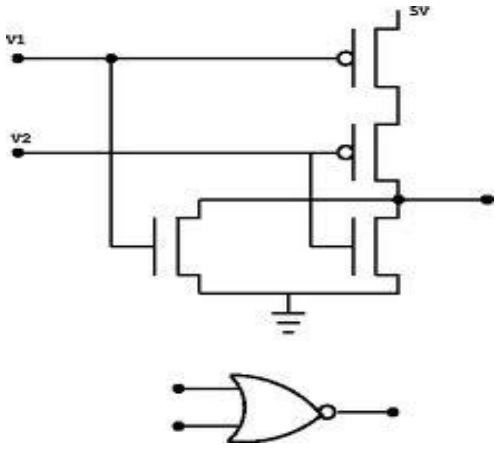


Fig. 4.1 CMOS 2 i/p NOR Gate

- The circuit consists of a parallel connected N-network and series connected complimentary P-network. The input voltage V_A and V_B applied to the gate of one N-MOS and one P-MOS transistor.
- When both the input voltages are low i.e. N-network is cut off and P-network creates a conducting path between the output node and supply voltage V_{DD}.

- When input A is low and B is high then M_1 remains in cut off and M_2 gets conduction of N-network and M_3 is in conduction state and M_4 is cut off, therefore the output develops across node 'C' is low.
- When both the inputs are high, then N-network creates a conducting path between the output node and ground and the P-network is cut off. The output develops is active low.

C-MOS NAND2 Gate:

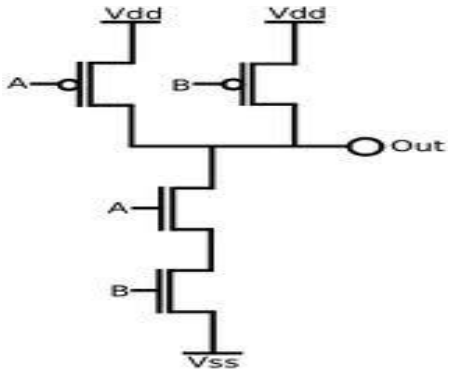


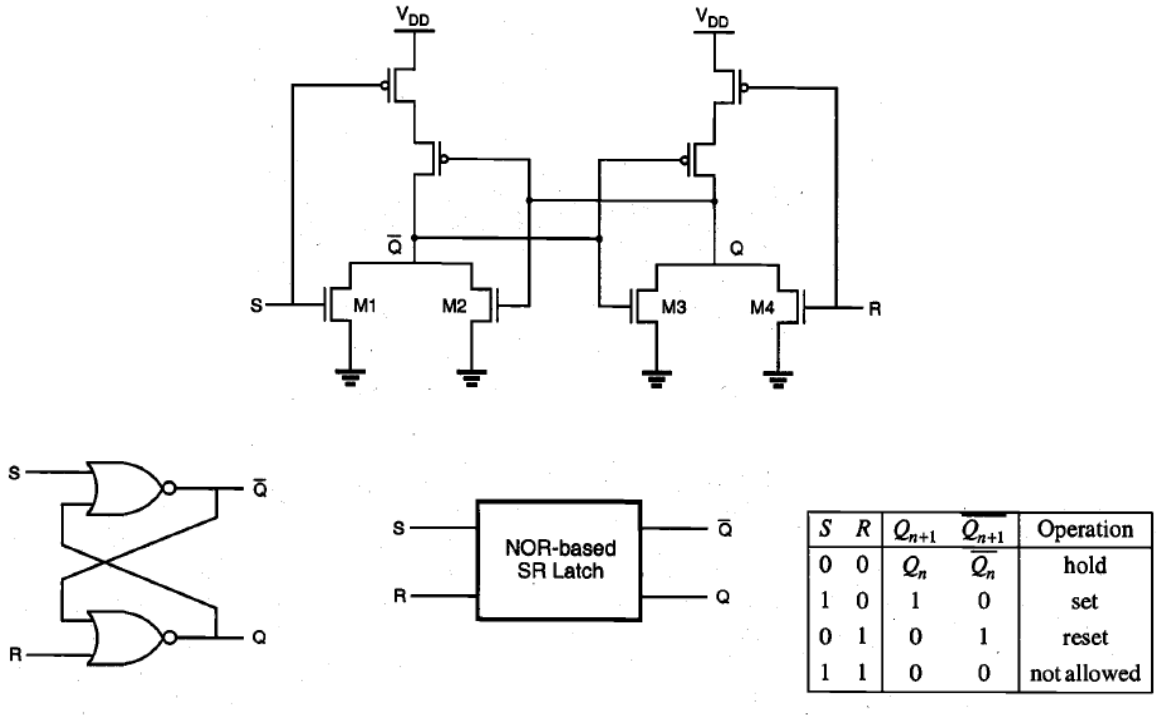
Fig. 4.2 CMOS 2 i/p NAND Gate

- It consists of two networks i.e. N-network and P-network.
- N-network consists of two series connected N-MOS transistors and P-network consists of two parallel connected P-MOS transistors.
- When both the inputs are active low, N-network is in cut off state and P-network is in conduction state, there the output is 1.
- When A is low and B is high the m3 gets conducted and m4 is in cut off state and the m2 of the N-network is cut off, therefore the output develops across point 'C' is high.
- When A is high and B is low then m4 gets conducted and m3 is in cut off state and m1 of N-network is in cut off state. Therefore the output develops across point 'C' is high.
- When both the inputs are high then N-network is in conduction state and P-network is in cut off state therefore, there is no path between Vcc and output. The output is low.

The SR Latch Circuit

The bi-stable element consisting of two cross-coupled inverters has two stable operating modes, or states. The circuit preserves its state (either one of the two possible modes) as long as the power supply voltage is provided; hence, the circuit can perform a simple memory function of *holding* its state. However, the simple two-inverter circuit examined above has no provision for allowing its state to be changed externally from one stable operating mode to the other. To allow such a change of state, we must add simple switches to the bi-stable

element, which can be used to force or trigger the circuit from one operating point to the other. Figure 6.7 shows the circuit structure of the simple CMOS SR latch, which has two such triggering inputs, S (set) and R (reset). In the literature, the SR latch is also called an SR flip-flop, since two stable states can be switched back and forth. The circuit consists of two CMOS NOR2 gates. One of the input terminals of each NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.

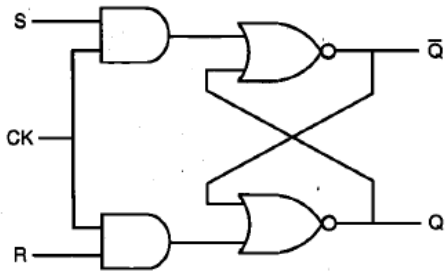


S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

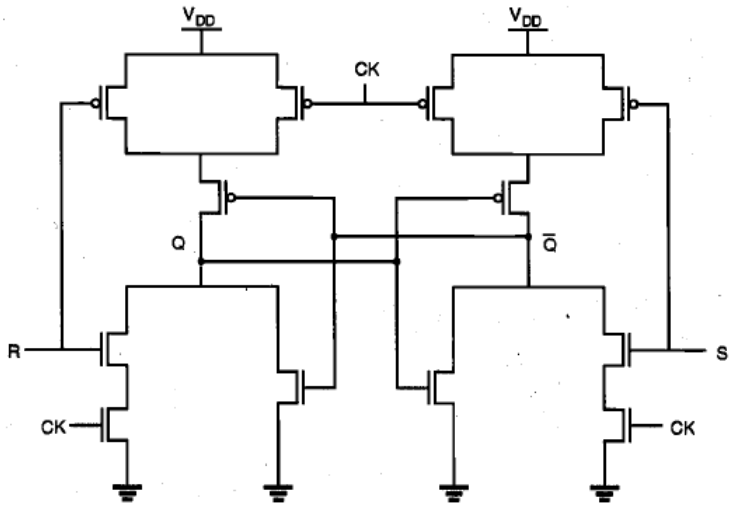
Fig. 4.3 Gate-level schematic and block diagram of SR latch with truth table.

Clocked SR Latch

All of the SR latch circuits examined in the previous section are essentially asynchronous sequential circuits, which will respond to the changes occurring in input signals at a circuit-delay-dependent time point during their operation. To facilitate synchronous operation, the circuit response can be controlled simply by adding a gating clock signal to the circuit, so that the outputs will respond to the input levels only during the active period of a clock pulse. For simple reference, the clock pulse will be assumed to be a periodic square waveform, which is applied simultaneously to all clocked logic gates in the system.



(Gate-level schematic of the clocked SR latch).



(CMOS clocked SR latch circuit.)

Fig. 4.4 Gate-level schematic and block diagram of clocked SR latch with truth table.

CMOS D-LATCH

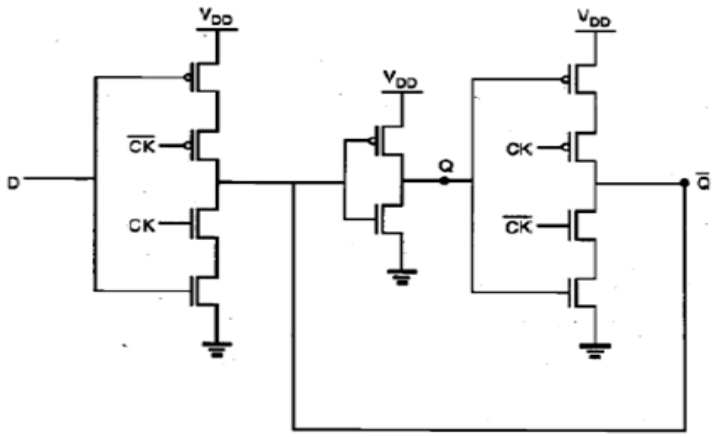


Fig. 4.5 CMOS D Latch

- The figure 4.5 shows the circuit of a CMOS D-Latch circuit. In this configuration the output follows the input with some propagation delay.
- With the active clock signal, when the input D is active high (Logic-1), the output terminal Q acquires the logic 1 state and the output Q' is at logic 0 level.
- When the clock signal is active and the input D is active low(Logic-0), the output terminal Q acquires the logic 0 state and the output Q' is at logic 1 level.

C-MOS Transmission Gate or Pass Transistor Logic

The C-MOS transmission gates consist of one N-MOS and one P-MOS transistor connected in parallel.

The gate voltage applied to these transistors is complimenting each other. The different represent of transmission gates are given below.

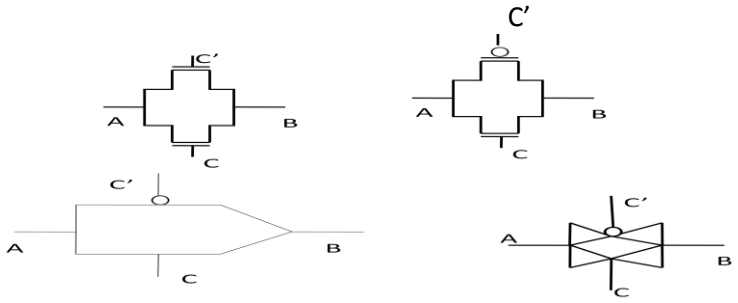


Fig. 4.6 Symbol of Transmission Gates

- The C-MOS transmission gate operates as bidirectional switch between node A and B which is controlled by signal C.
- If the control signal C is high i.e. equal to Vcc, both the transistors are turned ON and provide a low resistance path.
- If the control signal C is low, both the transistors will be in cut-off state and a open circuit exist between A & B. This condition is also known as high impedance state.
- The substrate of NMOS transistor must be connected to ground and the substrate of PMOS transistor must be connected to Vcc.
- There are 3 operating regions of transmission gates as given below

NMOS saturation	NMOS saturation	NMOS cutoff
PMOS saturation	PMOS linear	PMOS saturation
Region-1	Region-2	Region-1
0V	Vt	V_{dd}-V_t	V_{DD}

Dynamic Logic Circuits

A typical logic gate generates its output corresponding to the applied input voltage after a certain time delay and it can preserve its output level as long as power supply is available. This structure requires large number of transistors to implement a function and may cause a considerable time delay.

In contrast for high performance digital implementation where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits are extensively used. The operation of dynamic logic gates depends on temporary storage of charge parasitic load capacitances. This operational property requires periodic updating of load voltage levels as the capacitances cannot retain the charge definitely. So the dynamic logic circuits require periodic clock signals in order to control charge refreshing. The periodic clock signal also helps in synchronizing the operations of various circuit losses. This logic circuit implementation requires smaller silicon area than static logic circuits and less power consumption.

Basic Principle of Pass Transistor Circuit

The fundamental building block of N-MOS dynamic logic circuit consists of an N-MOS pass transistor driving the gate of another N-MOS transistor as shown in the figure below.

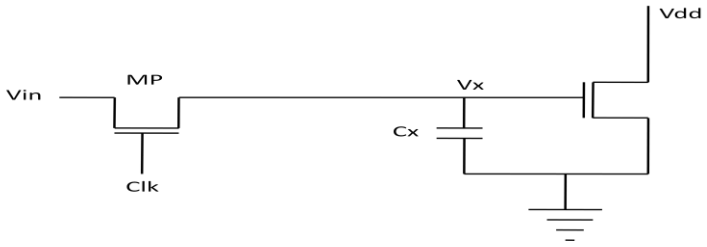


Fig. 4.7 Pass Transistor Logic Inverter

The pass transistor MP driven by the periodic clock signals and acts as an switch to either charge up or charge down the parasitic capacitance ‘Cx’ depending on the input signal Vin. When the clock signal is active and the input signal is at logic 1, the capacitor ‘Cx’ is charged up through the pass transistor MP. So the pass transistor MP provides the only current path to the intermediate capacitive node also known as soft node.

When the clock signal is active and input signal is at logic zero, the capacitor ‘Cx’ is charged down through the pass transistor MP. When the clock signals become inactive the pass transistor goes high and the charge stored in the parasitic capacitor ‘Cx’ continues to determine the output level of the inverter.

Semiconductor Memories

The semiconductor memories are generally used for storage of digital information. The semiconductor memories provide the facility of random data access and known as RAM. According to circuit configuration the RAM can be classified into two groups.

1- Dynamic RAM (DRAM)
2- Static RAM (SRAM)

In addition to above mentioned semiconductor memories another memory known as flash memories are also used in the digital circuits analogous to EEPROM. The following 3 criteria are important in designing semiconductor memories:

- Area efficiency of memory determines the number of bits stored per unit area.
- Speed of memory defining the access time of memory.
- Power consumption defining the power efficiency for low power operation.

Retrieving data from memory is called memory read and the time required to read from memory is called read-access time.

Similarly storing data into memory is called memory write and the time required to write into the memory is called write access time.

The row decoder is used to reduce the number of bits used for selecting the address of memory. The column decoder is used to select the number of bits to be retrieved as data.

Dynamic Random Access Memory (DRAM):-

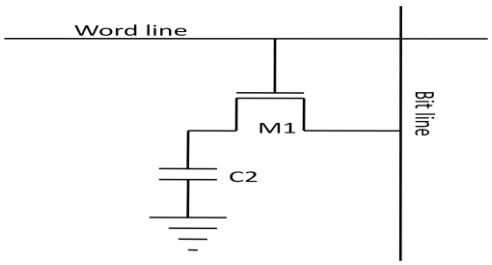


Fig. 4.8 Single bit DRAM Cell

- The figure 4.8 shows the equivalent circuit of one transistor DRAM cell. It consists of a capacitor (C*2*) and switching transistor. The data are stored on the capacitor as presence and absence of charge (logic 1 or 0).

- The stored charge is subject to gradual DL due to leakage current. So in order to keep the charge level constant continues refreshing signals are required.
- The data input lines are also known as bit lines and the read write select lines are also known as word line. Depending on the data on bit line and word line the respective data is stored from the capacitor depending on its charge level.
- The operation of one transistor DRAM all can be broadly classified into three sections, namely:-

1. Read
2. Write
3. Refresh

APPLICATION**:-**

Due to the low cost and high density fabrication the DRAM is quietly used for main memory in PC and main frame computers.

Static Random Access Memory (SRAM):-

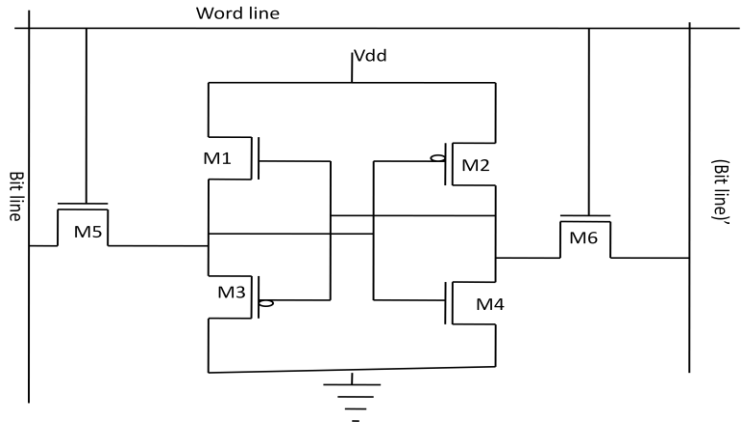


Fig. 4.9 Single bit SRAM Cell

- The figure 4.9 shows the circuit of a SRAM all having 6 transistors. Two CMOS inverters are connected back to back. Transistors (M1 & M3) and (M2 & M4) form the 2 inverters. Transistors M5 & M6 are used as a switch controlled by word line.
- To read data from cell, word line is enabled making transistors M5 & M6 ON. Hence the stored data is available in both the true and complemented form in the bit line and (bit line)' respectively.
- To write data into cell, again the word line is enabled and the data to be written is to be made available on the bit lines. The data is stored in the latch.

- The SRAM cells are most commonly used for cache memory in microprocessor mainframe computers and memory in hand held devices due to high speed and low power consumption.

Flash memory:-

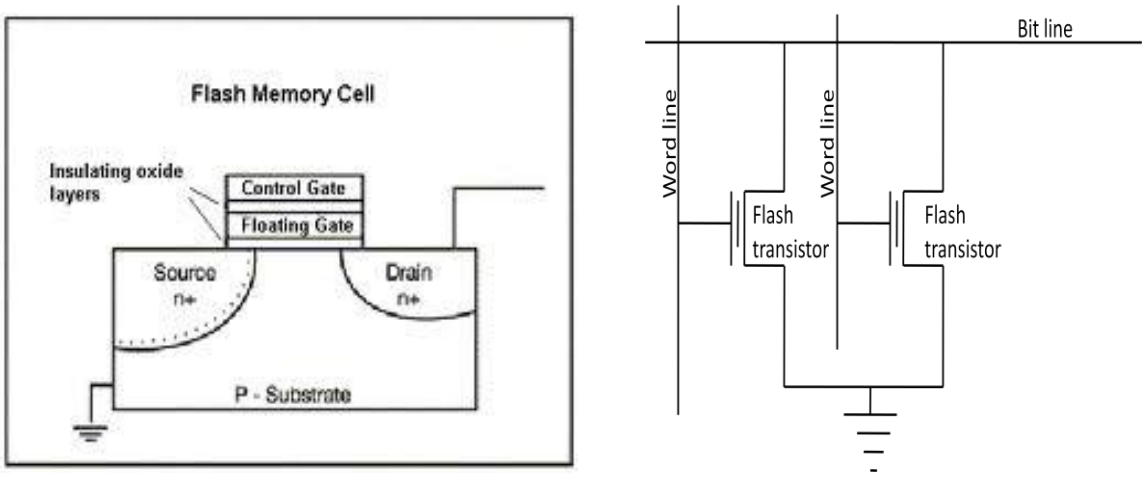


Fig. 4.10 Flash Memory Cell

- It is a non volatile computer storage chip that can be electrically erased and reprogrammed.
- It has higher speed of operation as compared to conventional EEPROM due to large block data operation.
- The flash memories are consists of one transistor with floating gate as shown in figure 4.10 above. Its threshold voltage can be charged repeatedly by applying electrical field to its gate terminal. The two states (Logic 0 and 1) can have two different threshold voltages corresponding to existence of charge at the floating gate.
- When the gate is connected to V_{DD} electrons are accumulated at the floating gate, resulting a logic one at the output.
- When the gate is connected to the ground potential, the charge on the floating gate discharges through the gate terminal resulting logic zero output.

Unit-5: System Design method & synthesis

7.1 Design capture tools, hardware definition languages such as VHDL and packages. Xlinx (introduction)

- Hardware description language (HDL): allows designer to specify logic function only. Then a computer-aided design (CAD) tool produces or synthesizes the optimized gates. Most commercial designs built using HDLs Two leading HDLs:

Verilog

  - Developed in 1984 by Gateway Design Automation
  - Became an IEEE standard (1364) in 1995

VHDL

- VHDL was originally developed at the behest of the U.S Department of Defense in order to document the behavior of the ASICs that supplier companies were including in equipment.
- The idea of being able to simulate the ASICs from the information in this documentation was so obviously attractive that logic simulators were developed that could read the VHDL files.
- The next step was the development of logic synthesis tools that read the VHDL, and output a definition of the physical implementation of the circuit.
- The initial version of VHDL, designed to IEEE standard 1076-1987, included a wide range of data types, including numerical (integer and real), logical (bit and Boolean), character and
- time, plus arrays of bit called bit vector and of character called string.

Standardization

- The IEEE Standard 1076 defines the VHSIC Hardware Description Language or VHDL. It was originally developed under contract F33615-83-C-1003 from the United States Air Force awarded in 1983 to a team with Intermetrics, Inc. as language experts and prime contractor, with Texas Instruments as chip design experts and IBM as computer system design experts.
- The language has undergone numerous revisions and has a variety of sub-standards associated with it that augment or extend it in important ways.

Design

- VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program

is used to test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a test bench.

- VHDL has constructs to handle the parallelism inherent in hardware designs, but these constructs (processes) differ in syntax from the parallel constructs in ADA (tasks). Like ADA, VHDL is strongly typed and is not case sensitive. In order to directly represent operations which are common in hardware, there are many features of VHDL which are not found in ADA, such as an extended set of Boolean operators including NAND and NOR. VHDL also allows arrays to be indexed in either ascending or descending direction; both conventions are used in hardware, whereas in ADA and most programming languages only ascending indexing is available.

Advantages

- The key advantage of VHDL, when used for systems design, is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires).
- Another benefit is that VHDL allows the description of a concurrent system. VHDL is a dataflow language, unlike procedural computing languages such as BASIC, C, and assembly code, which all run sequentially, one instruction at a time.
- A VHDL project is multipurpose. Being created once, a calculation block can be used in many other projects. However, many formational and functional block parameters can be tuned (capacity parameters, memory size, element base, block composition and interconnection structure).

Xilinx

- Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
- The Spartan-3 platform was the industry’s first 90nm FPGA, delivering more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.
- Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual

property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing.

- Xilinx's FPGAs have been used for the ALICE (A Large Ion Collider Experiment) at the CERN European laboratory on the French-Swiss border to map and disentangle the trajectories of thousands of subatomic particles. Xilinx has also engaged in a partnership with the United States Air Force Research Laboratory's Space Vehicles Directorate to develop FPGAs to withstand the damaging effects of radiation in space, which are 1,000 times less sensitive to space radiation than the commercial equivalent, for deployment in new satellites.
- The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families, which include up to two embedded IBM PowerPC cores, are targeted to the needs of system-on-chip (SoC) designers.
- Xilinx FPGAs can run a regular embedded OS (such as Linux or vxWorks) and can implement processor peripherals in programmable logic.
- Xilinx's IP cores include IP for simple functions (BCD encoders, counters, etc.), for domain specific cores (digital signal processing, FFT and FIR cores) to complex systems (multi-gigabit networking cores, the Micro Blaze soft microprocessor and the compact Picoblaze microcontroller). Xilinx also creates custom cores for a fee.
- The main design toolkit Xilinx provides engineers is the VIVADO Design Suite, an integrated design environment (IDE) with a system-to-IC level tools built on a shared scalable data model and a common debug environment. VIVADO includes electronic system level (ESL) design tools for synthesizing and verifying C-based algorithmic IP; standards based packaging of both algorithmic and RTL IP for reuse; standards based IP stitching and systems integration of all types of system building blocks; and the verification of blocks and systems. A free version WEBPACK Edition of VIVADO provides designers with a limited version of the design environment.
- Xilinx's Embedded Developer's Kit (EDK) supports the embedded PowerPC 405 and 440 cores (in VIRTEX-II Pro and some VIRTEX-4 and -5 chips) and the MICROBLAZE core. Xilinx's System Generator for DSP implements DSP designs on Xilinx FPGAs. A freeware version of its EDA software called ISE WEBPACK is used with some of its non-high-performance chips.

Designing FPGA Devices with VHDL

VHSIC Very high Speed Integrated Circuit) Hardware Description Language (VHDL) is a hardware description language for designing integrated circuits. Since VHDL was not originally intended as an input to synthesis, many VHDL constructs are not supported by synthesis tools. The high level of abstraction of VHDL makes it easy to describe the system-level components and test benches that are not synthesized. In addition, the various synthesis tools use different subsets of VHDL.

Using a Hardware Description Language (HDL) gives added flexibility in describing the design. Not all HDL code is optimized the same. How and where the functionality is described can have dramatic effects on end optimization. For example:

- Certain techniques may unnecessarily increase the design size and power while decreasing performance.
- Other techniques can result in more optimal designs in terms of any or all of those same metrics.

Design hierarchy is important in both the implementation of an FPGA and during interactive changes. Some synthesizers maintain the hierarchical boundaries unless you group modules together. Modules should have registered outputs so their boundaries are not an impediment to optimization. Otherwise, modules should be as large as possible within the limitations of your synthesis tool.

To meet timing requirements, you must set timing constraints in both the synthesis tool and the placement and routing tool. If you specify the desired timing at the beginning, the tools can maximize not only performance, but also area, power, and tool runtime.

This may result in a design that:

- Achieves the desired performance
- Is smaller
- Consumes less power
- Requires less processing time

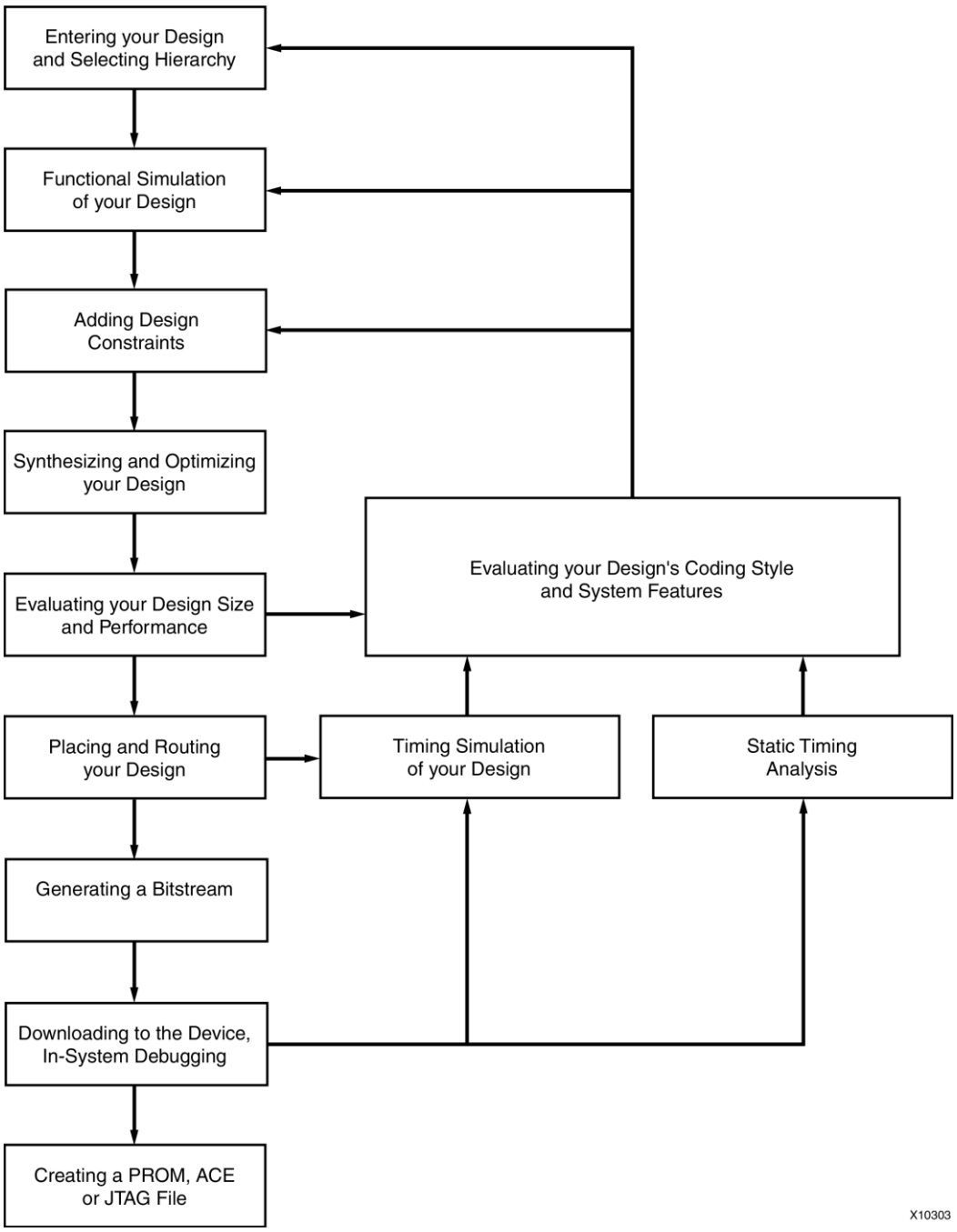


Fig. 5.1 FPGA Design Steps

Raspberry Pi

It is a series of small single-board computers (SBCs) developed in the United Kingdom by the Raspberry Pi Foundation in association with Broadcom. The Raspberry Pi project originally leaned towards the promotion of teaching basic computer science in schools and in developing countries. The original model became more popular than anticipated, selling outside its target market for uses such as robotics. It is widely used in many areas, such as for weather

monitoring, because of its low cost, modularity, and open design. It is typically used by computer and electronic hobbyists, due to its adoption of HDMI and USB devices.

The Raspberry Pi hardware has evolved through several versions that feature variations in the type of the central processing unit, amount of memory capacity, networking support, and peripheral-device support. The first generation (Raspberry Pi Model B) was released in February 2012.

In 2014, the Foundation released a board with an improved design, Raspberry Pi Model B+. These first generation boards feature ARM11 processors, are approximately credit-card sized and represent the standard mainline form-factor. The Raspberry Pi 2 was released in February 2015 and initially featured a 900 MHz 32-bit quad-core ARM Cortex-A7 processor with 1 GB RAM. Revision 1.2 featured a 900 MHz 64-bit quad-core ARM Cortex-A53 processor.

Raspberry Pi 3 Model B was released in February 2016 with a 1.2 GHz 64-bit quad core ARM Cortex-A53 processor, on-board 802.11n Wi-Fi, Bluetooth and USB boot capabilities. Raspberry Pi 4 Model B was released in June 2019 with a 1.5 GHz 64-bit quad core ARM CortexA72 processor, on-board 802.11ac Wi-Fi, Bluetooth 5, full gigabit Ethernet (throughput not limited), two USB 2.0 ports, two USB 3.0 ports, 2-8 GB of RAM, and dual-monitor support via a pair of micro HDMI (HDMI Type D) ports for up to 4K resolution.

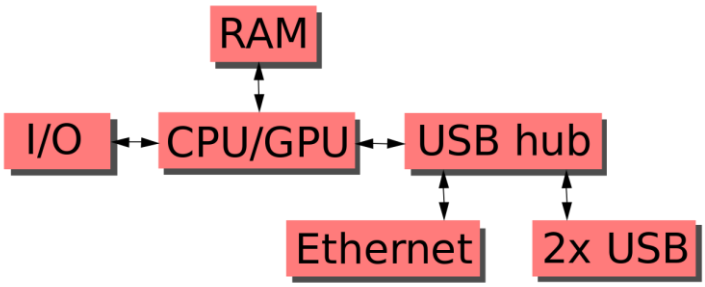


Fig 5.2 Raspberry – Pi Model

This block diagram describes models B, B+, A and A+. The Pi Zero models are similar, but lack the Ethernet and USB hub components. The Ethernet adapter is internally connected to an additional USB port. In Model A, A+, and the Pi Zero, the USB port is connected directly to the System on a Chip (SoC). On the Pi 1 Model B+ and later models the USB/Ethernet chip contains a five-port USB hub, of which four ports are available, while the Pi 1 Model B only provides two. On the Pi Zero, the USB port is also connected directly to the SoC, but it uses a micro USB (OTG) port. Unlike all other Pi models, the 40 pin GPIO connector is omitted on

the Pi Zero, with solderable through-holes only in the pin locations. The Pi Zero WH remedies this Processor speed ranges from 700 MHz to 1.4 GHz for the Pi 3 Model B+ or 1.5 GHz for the Pi 4; on-board memory ranges from 256 MB to 8 GB random-access memory (RAM), with only the Raspberry Pi 4 having more than 1 GB. Secure Digital (SD) cards in Micro SDHC form factor (SDHC on early models) are used to store the operating system and program memory, however some models also come with onboard EMMC storage and the Raspberry Pi 4 can also make use of USB-attached SSD storage for its operating system. The boards have one to five USB ports. For video output, HDMI and composite video are supported, with a standard 3.5 mm tip-ring sleeve jack for audio output. Lower-level output is provided by a number of GPIO pins, which support common protocols like I²C. The B-models have an 8P8C Ethernet port and the Pi 3, Pi 4 and Pi Zero W have on-board Wi-Fi 802.11n and Bluetooth.

Unit-6: Introduction to Embedded Systems

Embedded system overview:

Computing systems are everywhere. There is no surprise that millions of computing systems are built every year destined for workstations, mainframes and servers, Desktop computers Personal Computers.

The billions of computing systems are built every year for a very different purpose: they are embedded within larger electronic devices, repeatedly carrying out a particular function, often going completely unrecognized by the device's user. An embedded system is nearly any computing system other than a desktop, laptop, or mainframe computer.

Shortlist of embedded systems:-

Embedded systems are found in a variety of common electronic devices, such as:

1. Consumer electronics - cell phones, pagers, digital cameras, camcorders, videocassette recorders, portable video games, calculators, and personal digital assistants, etc.
2. Home appliances - microwave ovens, answering machines, thermostat, home security, washing machines, and lighting systems, etc.
3. Office automation -- fax machines, copiers, printers, and scanners, etc.
4. Business equipment - cash registers, curbside check-in, alarm systems, card readers, product scanners, and automated teller machines, etc.
5. Automobiles - transmission control, cruise control, fuel injection, anti-lock brakes, and active suspension, etc.

Characteristics of embedded systems:-

Embedded systems have several common characteristics:

1) SINGLE-FUNCTIONED: An embedded system usually executes only one program, repeatedly. For example, a pager is always a pager. A desktop system executes a variety of programs, Tike spreadsheets, word processors, and video games, with new programs added frequently.

2) TIGHTLY CONSTRAINED: All computing systems have constraints on design metrics. A design metric is a measure of an implementation's features, such as cost, size, performance, and power. Embedded systems often must cost just a few dollars, must be sized to fit on a single chip, must perform fast enough to process data in real-time, and must consume minimum power to extend battery life or prevent the necessity of a cooling fan.

3) REACTIVE AND REAL-TIME: Many embedded systems must continually react to changes in the system's environment, and must compute certain results in real time without delay. For example, a car's cruise controller continually monitors and reacts to speed and brake sensors. It must compute acceleration or decelerations amounts repeatedly within a limited time; a delayed computation result could result in a failure to maintain control of the car. A desktop system typically focuses on computations, with relatively infrequent (from the computer's perspective) reactions to input devices. In addition, a delay in those computations, while perhaps inconvenient to the computer user, typically does not result in a system failure.

Digital camera:

Consider the digital camera system as shown in the below figure.

- The A2D and D2A circuits convert analog images to digital and digital to analog respectively.
- The CCD preprocessor is a charge-coupled device preprocessor.
- The JPEG codec compresses and decompresses an image using the JPEG2 compression standard, enabling compact storage in the limited memory of the camera.
- The Pixel coprocessor aids in rapidly displaying images.
- The Memory controller controls access to a memory chip also found in the camera, while the DMA controller enables direct memory access without requiring the use of the microcontroller.
- The UART enables communication with a PC’s serial port for uploading video frames, while the ISA bus interface enables a faster connection with a PC's ISA bus.
- The LCD ctrl and Display ctrl circuits control the display of images on the camera's liquid-crystal display device.
- A Multiplier/Accumulator circuit assists with certain digital signal processing.
- The heart of the system is a microcontroller, which is a processor that controls the activities of all the other circuits. Each device as a processor designed for a particular task, while the microcontroller is a more general processor designed for general tasks.
- This example illustrates some of the embedded system characteristics described above.
- It performs a single function repeatedly. The system always acts as a digital camera, wherein it captures, compresses and stores frames, decompresses and displays frames, and uploads frames.
- It is tightly constrained. The system must be low cost since consumers must be able to

afford such a camera. It must be small so that it fits within a standard-sized camera. It must be fast so that it can process numerous images in milliseconds. It must consume little power so that the camera's battery will last a long time.

- This particular system does not possess a high degree of the characteristic of being reactive and real-time, as it only needs to respond to the pressing of buttons by a user, which even for an avid photographer is still quite slow with respect to processor speed.

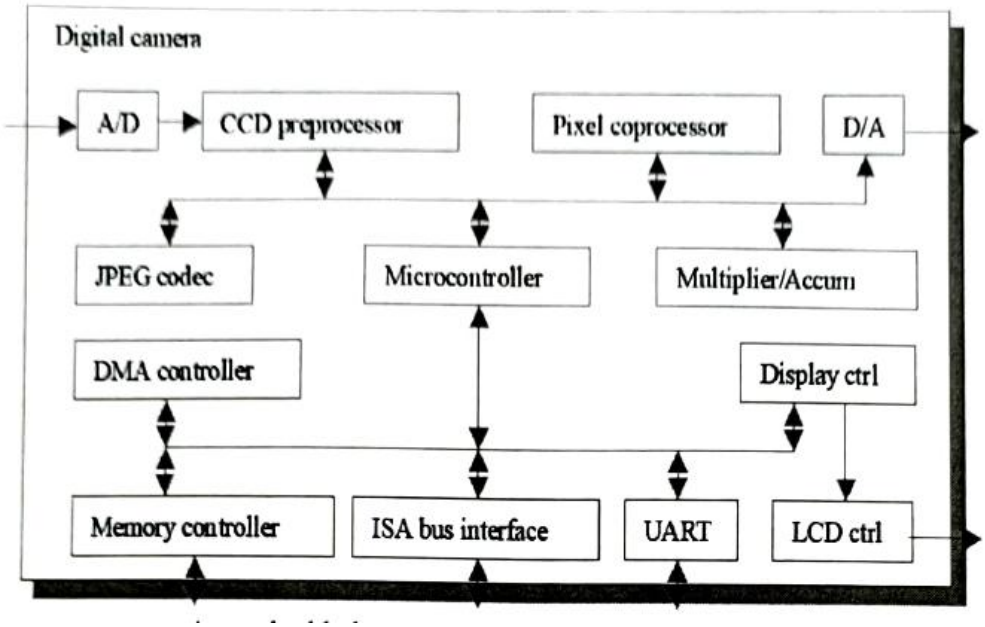


Fig. 6.1 Digital Camera Block Diagram

Embedded systems technologies:

- Technology as a manner of accomplishing a task, especially using technical processes, methods, or knowledge.
- There are three technologies
    1. Processor technologies
    2. IC technologies
    3. Design technologies

Processor technology:

According to the capability of any specific processor to address any specific function, there are 03 types of processors:

1. General Purpose Processor
2. Application Specific Processor
3. Single Purpose Processor

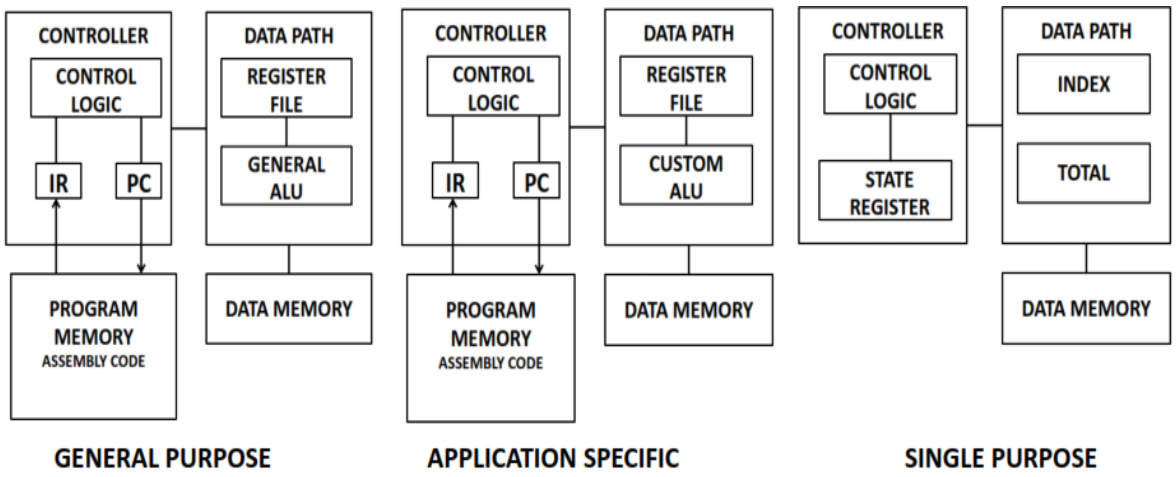


Fig. 6.2 Implementing desired functionality on different processor types

General Purpose Processors:-

- The general-purpose processor builds a device suitable for a variety of applications, to maximize the number of devices sold.
- One feature of such a processor is a program memory the designer does not know what Program will run on the processor, so the program cannot be build into the digital circuit.
- Another feature is a general data path - the data path must be general enough to handle a variety of computations, so typically has a large register file and one or more general-purpose arithmetic-logic units (ALUs).
- An embedded system simply uses a general purpose processor, by programming the processor's memory to carry out the required functionality.
- Using a general purpose processor in an embedded system may result in several design metric benefits.
  - Design time and NRF cost are low, because of the designer must only write a programme, but need not do any digital design.
  - Flexibility is high, because changing functionality requires only changing the programme.
  - Unit cost may be relatively low in small quantities, since the processor manufacturer sells large quantities to other consumers.
  - Performance may be fast for computation intensive applications, if using a fast processor, due to advance architecture features and leading edge IC technology.
- There are also some design metric drawbacks.

- Unit cost may be too high for large quantities.
- Performance may be slow for certain applications.
- Size and power may be large due to unnecessary processor hardware.

Single Purpose Processors Hardware:-

- A single-purpose processor is a digital circuit designed to execute exactly one program. For example, consider the digital camera. All of the components other than the microcontroller are single-purpose processors. The JPEG codec, for example, executes a single program that compresses and decompresses video frames.
- An embedded system creates a single-purpose processor by designing a custom digital circuit.
- Using a single-purpose processor in an embedded system results in several design metric benefits and drawbacks, which are essentially the inverse of those for general purpose processors.
- Performance may be fast, size and power may be small, and unit-cost may be low for large quantities, while design time and NRE costs may be high, flexibility is low, unit cost may be high for small quantities, and performance may not match general-purpose processors for some applications.

Application specific processors:-

- An application-specific instruction-set processor (or ASIP) can serve as a compromise between the other processor.
- An ASIP is designed for a particular class of applications with common characteristics, such as digital-signal processing. telecommunications, embedded control, etc.
- An ASIP in an embedded system can provide the benefit of flexibility while still achieving good performance, power and size.
- Such processors can require large NRE cost to build the processor itself.

Microcontrollers:

- A microcontroller is a microprocessor that has been optimized for embedded control applications.
- Such applications typically monitor and set numerous single bit control signals but do not perform large amount of data computations. Thus microcontrollers tend to have simple data paths that excel bit-level operations and reading and writing external bits.

- Furthermore, they tend to incorporate on the microprocessor chip compromise several components common in control applications like serial communication peripherals, times, counters, pulse width modulators and analog to digital converters. Such incorporation of peripherals enables single chip implementations and hence smaller and lower cost product.

Digital Signal Processing:-

- Digital-signal processors (DSPs) are a common class of ASIP.
- A DSP is a processor designed to perform common operations on digital signals, which are the digital encodings of analog signals like video and audio. These operations carry out common signal processing tasks like signal filtering, transformation, or combination.
- Such operations are usually math-intensive, including operations like multiply and add or shift and add.
- To support such operations, a DSP may have special purpose datapath components such as multiple-accumulator unit, which can perform a computation like T = T+ M[i]*k using only one instruction.

IC Technology:

- Every processor must eventually be implemented on an IC.
- An IC (Integrated Circuit), often called a "chip." is a Semiconductor device consisting of a set of connected transistors and other devices.
- A number of different processes exist to build semiconductors, the most popular of which is CMOS (Complementary Metal Oxide Semiconductor).

Semiconductor IC consist of numerous layers as shown in the figure given below.

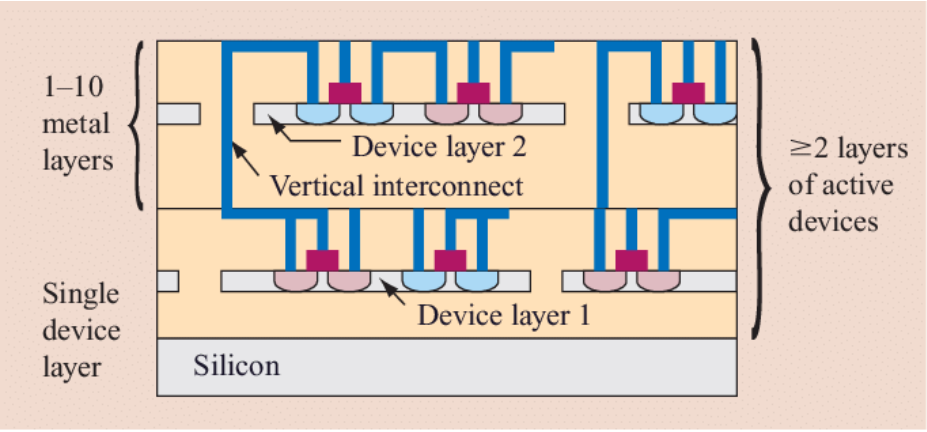


Fig. 6.3 Multi layer IC Structure

- The bottom layers may form the transistors. The middle layers may form logic gates. The top layers connect these gates with wires. These layers can be created by depositing photo-sensitive chemicals on the chip surface and then shining light through masks to change regions of the chemicals. A set of masks is often called a layout. The narrowest line that we can create on a chip is called the feature size.

Full Custom/VLSI:

- In a full-custom IC technology, we optimize all layers for our particular embedded system's digital implementation.
- Such optimization includes placing the transistors to minimize interconnection lengths, sizing the transistors to optimize signal transmissions and routing wires among the transistors.
- Once all the masks are completed, then we send the mask specifications to a fabrication plant that builds the actual ICs.
- Full-custom IC design, often referred to as VLSI (Very Large Scale Integration) design, has very high NRE cost and long turnaround times (typically months) before the IC becomes available, but can yield excellent performance with small size and power.
- It is usually used only in high-volume or extremely performance-critical applications.

Semicustom ASIC (Gate Array and Standard Cell):-

- In an ASIC (Application-Specific IC) technology, the lower layers are fully or partially built, leaving us to finish the upper layers.
- In a gate array technology, the masks for the transistor and gate levels are already built (i.e., the IC already consists of arrays of gates).
- The remaining task is to connect these gates to achieve our particular implementat1ion.
- In a standard cell technology. Logic level cells (such as an AND gate or an AND-OR-INVERT combination) have their mask portions pre-designed, usually by hand.
- Thus, the remaining task is to arrange these portions into complete masks for the gate level, and then to connect the cells.
- ASICs are by far the most popular IC technology as they provide for good performance and size with much less NRE cost than full custom IC's.

Programmable Logic Devices (PLDs):-

- In a PLD (Programmable Logic Device) technology, layers implement a programmable circuit, where programming has a lower level meaning than a software programme.
- The programming that takes place may consist of creating or destroying connections between wires that connect gates, either by blowing a fuse or setting a bit in a programmable switch.
- Small devices called programmers, connected to a desktop computer can typically perform such programming.
- PLD's are of two type, simple and complex. One type of simple PLD is a PLA (Programmable Logic Array), which consists of a programmable array of AND gates and a programmable array of OR gates.
- Another type is a PAL (Programmable Array Logic), which uses just one programmable array to reduce the number of expensive programmable components.
- One type of complex PLD, growing very rapidly in popularity over the past decade, is the FPGA (Field Programmable Gate Array), which offers more general connectivity among blocks of logic, rather than just arrays of logic as with PLAs and PALs and are thus able to implement far more complex designs. PLDs offer very low NRE cost and almost instant IC availability.
- They are typically bigger than ASICs, may have higher unit cost, may consume more power and may be slower (Especially FPGAs). They still provide reasonable performance, tough, so are especially well suited to rapid prototyping.

Arduino:

It is an open-source platform used for building electronics projects. Arduino consists of both a physical programmable circuit board (often referred to as a microcontroller) and a piece of software, or IDE (Integrated Development Environment) that runs on your computer, used to write and upload computer code to the physical board.

The Arduino platform has become quite popular with people just starting out with electronics, and for good reason. Unlike most previous programmable circuit boards, the Arduino does not need a separate piece of hardware (called a programmer) in order to load new code onto the board, you can simply use a USB cable.

Additionally, the Arduino IDE uses a simplified version of C++, making it easier to learn to program. Finally, Arduino provides a standard form factor that breaks out the functions of the micro-controller into a more accessible package.

The Arduino hardware and software was designed for artists, designers, hobbyists, hackers and anyone interested in creating interactive objects or environments. Arduino can interact with buttons/switches, LEDs, motors, speakers, GPS units, cameras, the internet, and even your smart-phone or your TV. This flexibility combined with the fact that the Arduino software is free, the hardware boards are pretty cheap, and both the software and hardware are easy to learn has led to a large community of users who have contributed code and released instructions for a huge variety of Arduino-based projects.

For everything from robots and a heating pad hand warming blanket to honest fortunetelling machines and even a Dungeons and Dragons dice-throwing gauntlet, the Arduino can be used as the brains behind almost any electronics project.

Books for Reference:

1. COMS Digital ICs –Analysis & Design –Sung Mo-Kang &Yussuf Leblebici, TMH.
2. VLSI Design AND EDA Tools by A. Sarkar,S.De,Chandran Kumar Sarkar –SCITECH
3. Embedded System Design –Frank Vahid& Tony Givargis-WILEY India.
4. VLSI Design by Sakthiver. R – S CHAND.
5. VHDL Programing by Example by Douglas L. Perry-TMH
6. VLSI Design – Debaprasad Das – OXFORD