Power Integrity in High-Speed PCB Design
Synopsis

An effective power distribution system is very important in high-speed printed circuit boards, which usually consist of large microprocessors and other high-speed silicon devices. Failure to design a stable power supply system in a PCB may result in impaired signals, jitter problem and violation of EMC regulations. This field of study is termed Power Integrity, and it has been catching up with Signal Integrity in terms of analysis, methodologies and techniques.

This course is specifically tailored for engineers intending to develop reliable power supply systems in high-speed PCBs. Relevant power supply issues, such as response of decoupling capacitors, impact of parasitic inductance, impedance profile of a power distribution system and ground bounce are discussed. Lectures are interlaced with background theories, real-life examples and hands-on practical to maximize learning effectiveness.

What You Will Learn

- Importance of power decoupling
- Factors that affect mounting inductance of capacitors
- Power integrity analysis - IR drop, ac noise and decoupling analysis
- Impedance profile of a power distribution network
- Methods for reducing ground bounce and simultaneous switching noise
- Practical layout techniques for achieving good power integrity in high-speed PCBs.

Who Should Attend

This course is particularly suited for engineers responsible for designing and verifying power distribution systems in high-speed PCBs.

Prerequisite

Technical background or working experience with PCB layout and analysis for high-speed circuits.

Course Methodology

This course is presented in a workshop style with example-led lectures interlaced with hands-on practical for maximum understanding.

Course Duration

3 day(s), 9am - 5pm

Course Structure
Power Decoupling

- Power supply system in a PCB
- Power supply and SI & EMC
- Impact of power supply noise
- Challenges on power supply
- The purpose of power decoupling
- Basic design rules for making a good power system
- Transient power supply currents in a logic gate

Capacitors

- Functions, characteristic, ESR, ESL and self-resonant frequency of capacitors
- Package size and ESL
- The impact of ESL to capacitor performance
- Different types of capacitors (decoupling, planar, bulk, 3-pin capacitors)
- Effective planar capacitance area

Mounting Inductance of Capacitors

- Different types of mounting inductance for capacitors
- Capacitor trace inductance
- Via pair loop inductance
- Spreading inductance
- How PCB stack-up configuration affects inductance
- When does capacitor location matter
- Factors beyond board level
- Impact of package inductance

Power Integrity Analysis

- What is power integrity analysis
- IR drop analysis
- Noise analysis
- Decoupling analysis
- Power-ground plane resonance
- Voltage fluctuation and target impedance
- Transient current and target impedance

Impedance Profile of a Power Distribution Network

- What is a Power Distribution Network (PDN)
- Impedance profile of a PDN
- Anti-resonance in parallel connected capacitors
- Methods to minimize anti-resonance
- How many capacitors are needed for a PDN
- Should use capacitors with same or different values for a PDN
- Interaction between decoupling capacitor with planar capacitor
Ground Bounce, Power Sag and Simultaneous Switching Noise (SSN)

- Mechanism of ground bounce, power sag and SSN
- How ground bounce causes logic errors
- How SSN is coupled to signal
- Method for reducing ground bounce and power sag

PDN & EMI

- PDN related noise sources that may cause EMI problems
- How decoupling capacitors reduce radiated emission

Design and Layout Techniques for Good Power Integrity

- Important design guidelines for a PDN
- PCB stack-up configurations that provide good power decoupling
- Capacitor mounting methods that will minimize parasitic inductance
- Power entry filter layout techniques
- DC-DC converter layout techniques
- Decoupling capacitors mounting techniques on high current termination islands
- Power and ground vias arrangements that help to minimize loop area
- Why differential signaling can minimize common-impedance coupling
- Techniques for isolating quiet and noisy ground islands
- Relationship between decoupling capacitors and return current design

Hands-on Session:
Demonstrating power integrity problem via measurement
AC noise, anti-resonance frequency, impedance profile simulation
PCB design exercise on Power Integrity

**Course Instructor(s)**

**Mr Chai Ched Chang**

Mr Chai Ched Chang received his B.Eng (Hons) from University of Malaya, Malaysia, and M.EngSc from Multimedia University, Malaysia. He was one of the pioneer researchers on signal integrity (SI) in Multimedia University. From 1998 to 2001, he had accomplished research projects in crosstalk, PCB modelling using 3-D full-wave Finite-Difference Time-Domain (FDTD) method, and lab measurement. His research outcome was published in reputable international conference and journal through Multimedia University.

Mr Chai then began his career as a signal integrity engineer in 2001 at Ultimate Technologies Asia Sdn Bhd, and specialized in designing high-speed PCB. He had delivered many consumer electronics PCB designs, where he is specifically experienced in resolving SI issues associated with high-speed memory (SDRAM, DDR, DDR2, DDR3, etc.), differential signaling (LVDS, HDMI, USB, PCI Express, Ethernet, etc.), and other digital interfaces (FPGA interface,
FLASH memory, video bus, ADC & DAC, etc.). He also has vast experience in making PCB stack-up, and high-speed signal simulation and analysis.

In 2012, Mr Chai left Ultimate Technologies Asia as Chief Operating Officer and Chief Technical Officer, and started his company, iRtec Consulting Sdn Bhd. With over two decades of combined experience in both research and industry, he continues to strive to provide the best signal integrity consultation service with the vision to help his clients design products that meet their stringent quality requirements and shorten their product development cycle.
Administrative Details

Programme Logistics

Duration: 3 day(s), 9am - 5pm  
Date: 22 - 24 Jul 19  
Venue: Dream Catcher Consulting Sdn Bhd, Penang

Morning break, lunch and tea break will be provided throughout the course duration. Course Manual and Certificate of Attendance will be provided.

Your Investment

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<th>Condition</th>
<th>Price per Pax</th>
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<tr>
<td>Regular fee</td>
<td>RM3,420.00</td>
<td>RM205.20</td>
<td>RM3,625.20</td>
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<tr>
<td>Early bird discount for registration before 24-Jun-2019. N/A for SBL KHAS</td>
<td>RM3,110.00</td>
<td>RM186.60</td>
<td>RM3,296.60</td>
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<td>Group discount for every 3 pax registered, receive 1 complimentary seat</td>
<td>RM3,420.00</td>
<td>RM205.20</td>
<td>RM3,625.20</td>
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Additional cost may incur for customization or extra material request. Course fee is 100% claimable from PSMB (SBL scheme) in accordance to PSMB guidelines.

3 Easy Steps to Register

- **Phone** +604 640 7111 / 7112
- **Fax registration form** to +604 640 7110
- **Email registration form** to register@dreamcatcher.asia
Method of Payment

Crossed cheque / bank draft made in favour of DREAM CATCHER CONSULTING SDN BHD.
Registration form
together with payment to be couriered to :

Dream Catcher Consulting Sdn Bhd
303-4-5 & 303-4-6
Block B, Krystal Point
Jln Sultan Azlan Shah
11900 Sg Nibong
Penang, Malaysia

Payment must be received no later than 10 working days before the course commences. An
undertaking may be accepted in cases where payment is delayed. However all payments must
be made before the course commences.
Closing registration date is 08-Jul-2019.

Refund and Cancellation

Fees will only be refunded in full for cancellation received in writing more than 10 working days
prior to the commencement date. Substitute attendee(s) will be accepted at no extra charge.

Disclaimer

Dream Catcher Consulting Sdn Bhd reserves the right to change the instructors, date and to
vary/cancel the programme should unavoidable circumstances arise. All effort will be taken to
inform participants of the changes. Upon sending the registration form, you are deemed to
have read and accepted the terms.

Enquiries

call us at +604 640 7111 / 7112 or email us at enquiry@dreamcatcher.asia
### Registration Form

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<th>No.</th>
<th>Name</th>
<th>Job Title</th>
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**Total Amount**

*(Emails are required to ensure notification of any changes reach the participant)*

**Submitted by:**

- **Company Name:**
- **Company Address:**
- **Contact Person:**
- **Designation:**
- **Phone:**
- **Email:**

*Please complete this form with an authorised signature below and fax to fax registration form to +604 640 7110 or email to email registration form to register@dreamcatcher.asia. Call us at phone +604 640 7111 / 7112 for any enquiry.*

**Authorised Signature:**

*Please print full name (authorised signature) if you submit via email*

- **Name:**
- **Designation:**
- **Date:**

*This registration is invalid without a signature. Payment must be made no later than 10 working days before the course commences. An undertaking may be accepted in cases where payment is delayed, however all payment must be made before the course commences. Participants who registered but did not attend will be invoiced accordingly. Fees will only be refunded in full for cancellation received in writing more than 10 working days prior to the commencement date. Substitute attendee(s) will be accepted at no extra charge.*

*Please send payment with this form to*

Dream Catcher Consulting Sdn Bhd

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- **Jln Sultan Azlan Shah**
- **11900 Sg Nibong**
- **Penang, Malaysia**

*Enclosed cheque/bank draft no __________________ made in favour of DREAM CATCHER CONSULTING SDN BHD*