Fundamentals of Semiconductor Device Test Methodology

Training Programme
by
Dream Catcher Consulting Sdn Bhd

01 - 02 Aug 19
Dream Catcher Consulting Sdn Bhd, Penang

303-4-5 & 303-4-6 Block B, Krystal Point
Jln Sultan Azlan Shah 11900 Sg Nibong Penang, Malaysia
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**Synopsis**

Semiconductor test is one of important process in manufacturing semiconductor devices. It is important for the semiconductor test engineers to understand the fundamentals of the test methodology in order to design the most optimized test plan for the IC chip to improve the throughput, reduce significant cost, boost the process yield, minimize waste from yield loss, and at the same time put the quality at the highest priority.

The knowledge will also enable the test engineers to look for advanced techniques in testing such as multiple DUT testing, parallel testing, looping test, DUT re-socketing, etc. to increase the productivity and improve the UPH. In addition, the engineers can use the knowledge to design a test program that can perform product characterization based on the criteria set by the quality engineers. The understandings of the test methodology will also help a test Engineer to design a test module that is able to catch a process excursion either in assembly or wafer fab process to catch any quality issue, product defect, assembly problem, etc.

Any excursions for example can be detected and automatic triggering mechanisms such as SMS can be implemented in real time for the Engineers to put the CA as soon as possible. This knowledge will also help the test engineer team to put optimized TTR process by looking at the statistics on the most stable parameters that can be eliminated in order to speed up the test time.

In a nutshell, this training is very suitable for semiconductors test/quality/product engineers who want to learn the basic test methodology before designing the real test program for their products.

**What You Will Learn**

- Semiconductor manufacturing process from fab to packaging
- The probing and test process
- Different probe and test stations and the data structure
- Basic test methodology of developing a final test process
- Load board/test board design for testability
- Different handlers available in semiconductor industry today
- Fundamentals of multiple testing and re-socketing
- Hands on experience on writing a test program for a device

**Who Should Attend**

Manufacturing, product, test, and QA technicians and engineers who need to develop or modify test plan for running semiconductor device test.

**Prerequisite**

Participants should have at least a basic knowledge in probing, test operations, and basic electronics.

**Course Methodology**
The course is practically oriented with numerous examples and lab works using modular test equipment such as multimeter, oscilloscope, network analyzer, etc. in order to help the attendees to understand the course. Participants are divided into groups with a set of equipment to perform the test development process. At the end, participants will submit the test-plan proposal in a written report.

**Course Duration**

2 day(s), 9am - 5pm

**Course Structure**

**Day 1**

**Introduction to Semiconductor Manufacturing**

- Fundamentals of FAB process – types of FAB process: ABP, SiGe, etc.
- FOL semiconductor flow - backlapping, sawing, inking
- Probing process – type of probers: Electroglas, Tarasemi, probe data format
- Fundamentals of the EOL process – DA, WB, PKG, SGL
- Normal visuals reject at the visual inspection process

**Fundamentals of the BE Testing**

- Testing process – type of testers, test data format
- Handlers technology – types of handlers: Delta, AdvanTest, Exatron, Unisys, dual, triple, quad, etc. Multiple testing, resocketing, etc.
- Contactor technology – types of material: beryllium copper with gold plated metal fingers, spring loaded with gold plated, multiple layers, vertical, horizontal, etc. 200K contacts life-span
- DataBase technology to store probe and test data – MySQL, Oracle, PostGres, MongoDB, etc.
- How the data network being layout
- Tools to analyze the test data: Power BI, JMP, Jwarp

**Fundamentals of the Test Methodology for a Semiconductor Device**

- Introduction to device test specs
- Basics of the test plan – sequence of test modules.
- Types of test – DC, functional, digital IC, RF microwave, special test, binning
- DC tests
  - Shorts test
  - Opens test
  - Leakage test
  - Device orientation test
- Functional tests
  - Functionality of a device at given specs
  - Tested cover all geography on earth – room(25°C), cold(-5°C), hot(80°C)
  - Tested for military and space conditions – (100°C, -20°C, 2G drop, etc.)
  - Tested after stress test, eg. 2XIR, 3XIR, etc. – screen manufacturing defect, T0 failures, etc.
- The digital IC testing
  - Setup time
  - Hold time
- Delay time
- Logical patterns testing
- Special/extended tests
  - P1dB
  - G1dB
- Introduction to binning
  - Binning because of device speed in functionality
  - Binning of higher gain/beta value
  - Binning of special tests, eg. G1dB, P1dB
- A complete semiconductor test system – handler, tester, T&R machine.
- ESD controls in a manufacturing line – grounding system, etc.

**Day 2**

**Understanding the Device Under Test (DUT)**
- Understand the function of the DUT (case study: op-amp)
  - Voltage amplifier
  - Inverter
- Test specs for the given product
  - DC specs
  - AC specs
  - Binning requirements, eg. on open loop gain (Aol)
- Test plan – DC tests, functional test, gain test, etc,

**Practical Sessions**
The development of the test methodology
- Shorts test
- Opens test
- leakage test
- RF test – voltage gain
- Special test – P1dB, G1dB, etc.
- Binning test based on open loop gain, etc.
- Rewrite all the test plans on papers and submit to instructor for evaluation

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**Course Instructor(s)**

**Mr Ahmad Nasser Bin Osman**

Ahmad graduated from UKM (Universiti Kebangsaan Malaysia) in 1992 in the field of Electronics Engineering. He was one of seven ICI scholarship holders throughout Malaysia during his tenure year. Ahmad also holds a Master degree in Electronics from USM in 2011.

Ahmad joined Intel in November, 1992 as a 486 Product Test Engineer and was trained to program the Trillium tester using Pascal for two years. In 1994, he was promoted to Pentium Test Engineer and was sent to San Jose for a year to learn the software and hardware for the Schlumberger S9K FX/GX system that was used for Pentium, which ran in HP Unix and used C language as the platform. Upon certified, he was sent to Beaverton, Intel Oregon to perform silicon debug for the Pentium II using S9K FX testers. In 1995, Ahmad was promoted as Senior Pentium Product Test Engineer in Intel.

In March, 1997 Ahmad was offered a position as the Specialist Test Engineer in Product
Engineering department in WSD (Wireless Semiconductor Division in HP) for a series of RFIC products such as power modules, Fbar chips, power transistors, VCO, etc. Ahmad needed to observe production testing lines in Unisem, Carsem, Isotech, ASEM, ASEK, Inari, and others. Ahmad also engaged in validating product returns from customers including RFIC testing and FA performed in the lab.

In July, 1998 he was sent for one year in San Jose to learn on the SDI (Strategic Data Integration) software, which was developed by HP Software Engineers to analyze wafer probe data in San Jose plant. He studied the software and modified it to suit the backend process in HP. After he returned, he worked with the production test team to install the SDI system on various production lines to process and analyze the probe and test data.

In November, 2015 Ahmad was promoted to Principal Engineer in Avago (which spun from HP), which specialized in designing the Data Automation System for probe and test operations worldwide. Ahmad mastered the Perl language and focused on the development of the DB system for Avago/Agilent and Broadcom (which spun from Avago) to manage the probe and test data files from subcons such as Avago wafer fab in San Jose and Inari Assembly plant in Penang. Ahmad left Broadcom in 2017 to explore as freelance trainer in DreamCatcher and other institutions.

Ahmad stays in Penang with five children and enjoys travelling. He is also good in table tennis and badminton and won the closed HP table-tennis men singles twice during his service periods.
**Administrative Details**

**Programme Logistics**

**Duration:** 2 day(s), 9am - 5pm  
**Date:** 01 - 02 Aug 19  
**Venue:** Dream Catcher Consulting Sdn Bhd, Penang

Morning break, lunch and tea break will be provided throughout the course duration. Course Manual and Certificate of Attendance will be provided.

**Your Investment**

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<th>Type</th>
<th>Condition</th>
<th>Price per Pax</th>
<th>SST (6%)</th>
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<tr>
<td>Regular Fee</td>
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<td>RM2,420.00</td>
<td>RM145.20</td>
<td>RM2,565.20</td>
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<td>Early Bird Discount</td>
<td>for registration before 04-Jul-2019. N/A for SBL KHAS</td>
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<td>RM132.00</td>
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<td>Group Discount</td>
<td>For every 3 pax registered, receive 1 complimentary seat</td>
<td>RM2,420.00</td>
<td>RM145.20</td>
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Additional cost may incur for customization or extra material request. Course fee is 100% claimable from PSMB (SBL scheme) in accordance to PSMB guidelines.

**3 Easy Steps to Register**

- **Phone** +604 640 7111 / 7112
- **Fax registration form** to +604 640 7110
- **Email registration form** to register@dreamcatcher.asia
Method of Payment

Crossed cheque / bank draft made in favour of DREAM CATCHER CONSULTING SDN BHD. Registration form together with payment to be couriered to:

Dream Catcher Consulting Sdn Bhd
303-4-5 & 303-4-6
Block B, Krystal Point
Jln Sultan Azlan Shah
11900 Sg Nibong
Penang, Malaysia

Payment must be received no later than 10 working days before the course commences. An undertaking may be accepted in cases where payment is delayed. However all payments must be made before the course commences. Closing registration date is 18-Jul-2019.

Refund and Cancellation

Fees will only be refunded in full for cancellation received in writing more than 10 working days prior to the commencement date. Substitute attendee(s) will be accepted at no extra charge.

Disclaimer

Dream Catcher Consulting Sdn Bhd reserves the right to change the instructors, date and to vary/cancel the programme should unavoidable circumstances arise. All effort will be taken to inform participants of the changes. Upon sending the registration form, you are deemed to have read and accepted the terms.

Enquiries

call us at +604 640 7111 / 7112 or email us at enquiry@dreamcatcher.asia
## Registration Form

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Job Title</th>
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(Emails are required to ensure notification of any changes reach the participant)

### Submitted by:

- **Company Name:**
- **Company Address:**
- **Contact Person:**
- **Designation:**
- **Phone:**
- **Email:**

Please complete this form with an authorised signature below and fax to fax registration form to +604 640 7110 or email to email registration form to register@dreamcatcher.asia. Call us at phone +604 640 7111 / 7112 for any enquiry.

- **Authorised Signature:**

  * Please print full name (authorised signature) if you submit via email

- **Name:**
- **Designation:**
- **Dept:**
- **Date:**

This registration is invalid without a signature. Payment must be made no later than 10 working days before the course commences. An undertaking may be accepted in cases where payment is delayed. However all payment must be made before the course commences. Participants who registered but did not attend will be invoiced accordingly. Fees will only be refunded in full for cancellation received in writing more than 10 working days prior to the commencement date. Substitute attendee(s) will be accepted at no extra charge.

Please send payment with this form to

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Enclosed cheque/bank draft no ______________________ made in favour of DREAM CATCHER CONSULTING SDN BHD